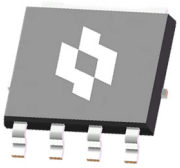
Product Summary

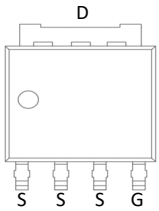
V_{DS}	$R_{DS(ON)_TYP}$	I_{D_MAX}
60 V	2.3 mΩ @V_{GS} = 10V	152 A

LFPAK5060

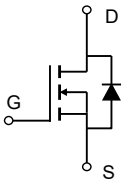


Top View

Bottom View



PIN Configuration
(Top View)



Schematic Diagram

Sinesemi Automotive MOSFET

AEC Qualified RoHS HALOGEN FREE

Features

- N-Channel Enhancement Mode - Standard Level
- AEC-Q101 Qualified, PPAP Capable
- 175°C Operating Temperature
- 100% ΔVDS & UIS & R_g Tested

Application

- General Automotive Applications

Mechanical Data

- Green Molding Compound
- Moisture Sensitivity: Level 1 per J-STD-020
- UL Flammability Classification Rating 94V-0

Ordering Information

Orderable Part Number	Package Type	Device Marking	Form	Quantity (pcs)
SMT6002BHFP5Q	LFPAK5060	6002BHQ	13" Tape&Reel	5,000

Maximum Ratings (@ T_C = 25°C, unless otherwise specified.)

Parameter		Symbol	Value	Unit
Drain - Source Voltage		V_{DS}	60	V
Gate - Source Voltage		V_{GS}	±20	V
Continuous Drain Current (V_{GS} = 10V) (1)	T_C = 25°C	I_D	152	A
	T_C = 100°C		107	A
Pulsed Drain Current (2)		I_{DM}	572	A
Single Pulse Avalanche Energy (3)		E_{AS}	360	mJ
Single Pulse Avalanche Current (L= 0.1mH)		I_{AS}	53	A
Power Dissipation	T_C = 25°C	P_D	125	W
	T_C = 100°C		63	W
Junction & Storage Temperature Range		T_J, T_{STG}	-55 ~ +175	°C

Thermal Characteristics

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance, Junction-to-Ambient (4)	$R_{\theta JA}$	35	45	°C/W
Thermal Resistance, Junction-to-Case (5)	$R_{\theta JC}$	0.95	1.2	°C/W

Electrical Characteristics (@ T_J = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Off Characteristics (6)						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60V, V_{GS} = 0V	-	-	1.0	μA
		T_J = 125°C	-	-	100	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V	-	-	±100	nA
On Characteristics (6)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250μA	2.0	3.0	4.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 20A	-	2.3	2.8	mΩ
Forward Transconductance	g_{fs}	V_{DS} = 5.0V, I_D = 20A	-	39	-	S
Diodes Forward Voltage	V_{SD}	I_S = 2.0A, V_{GS} = 0V	-	0.7	1.2	V
Dynamic Characteristics (7)						
Input Capacitance	C_{iss}	V_{DS} = 30V, V_{GS} = 0V, f = 1MHz	-	2717	3532	pF
Output Capacitance	C_{oss}		-	1089	1416	pF
Reverse Transfer Capacitance	C_{rss}		-	48	96	pF
Gate Resistance	R_g	V_{GS} = 0V, V_{DS} = 0V, f = 1MHz	-	1.2	-	Ω
Switching Characteristics (7)						
Turn-On DelayTime	$t_{d(on)}$	V_{GS} = 10V, V_{DS} = 30V I_D = 20A, R_{GEN} = 3.0Ω	-	7.2	-	ns
Rise Time	t_r		-	11	-	ns
Turn-Off DelayTime	$t_{d(off)}$		-	24	-	ns
Fall Time	t_f		-	11	-	ns
Gate Charge Characteristics (7)						
Total Gate Charge (V_{GS} = 10V)	Q_g	V_{DS} = 30V, I_D = 20A V_{GS} = 10V	-	45	59	nC
Total Gate Charge (V_{GS} = 6.0V)	Q_g		-	28	36	nC
Gate-Source Charge	Q_{gs}		-	11.6	17.4	nC
Gate-Drain Charge	Q_{gd}		-	11.5	17.3	nC
Gate Plateau Voltage	$V_{plateau}$		-	4.7	-	V
Drain-Source Diode Characteristics (7)						
Body Diode Reverse Recovery Time	t_{rr}	I_F = 20A, dI/dt = 100A/μs, T_J = 25°C	-	43	-	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	59	-	nC
Diode Forward Current	I_S	T_C = 25°C	-	-	152	A

Notes:

1. This current is chip limited, which is calculated based on Rthjc.
2. This current is calculated on single pulse with 10μs Single Pulse.
3. Defined by design, not subject to production test, E_{AS} condition: T_J=25°C, V_{DD}=30V, V_{GS}=10V, L=1.0mH.
4. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
5. Thermal resistance from junction to the exposed drain pad.
6. Short duration pulse test used to minimize self-heating effect.
7. Defined by design, not subject to production.

Typical Electrical and Thermal Characteristics

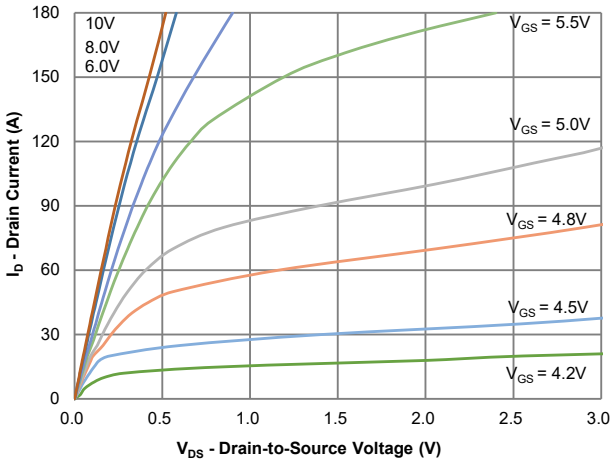


Figure 1: Output Characteristics

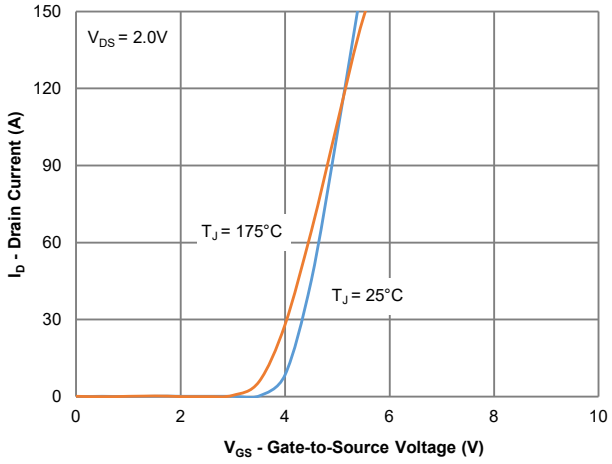


Figure 2: Transfer Characteristics

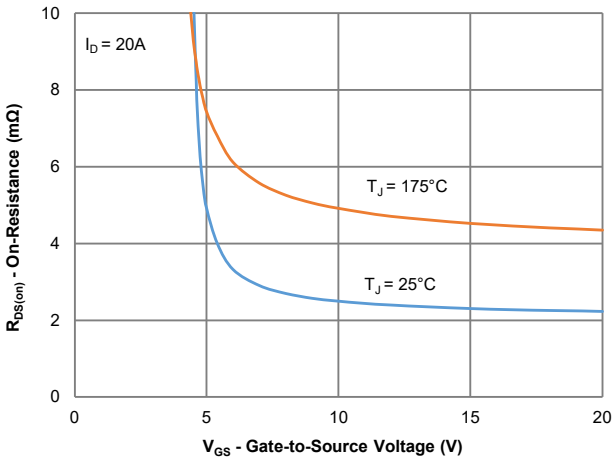


Figure 3: On-Resistance vs. Gate-Source Voltage

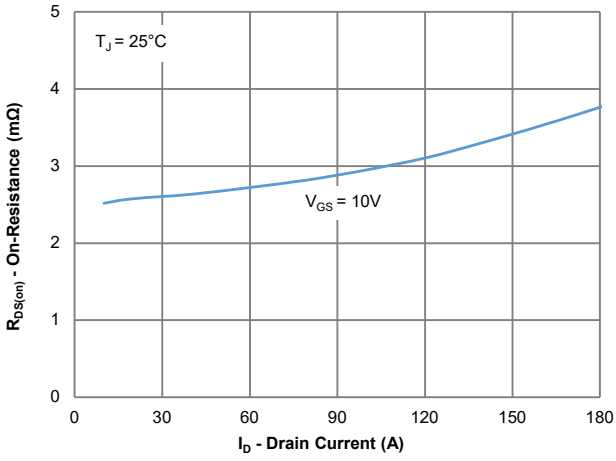


Figure 4: On-Resistance vs. Drain Current and Gate Voltage

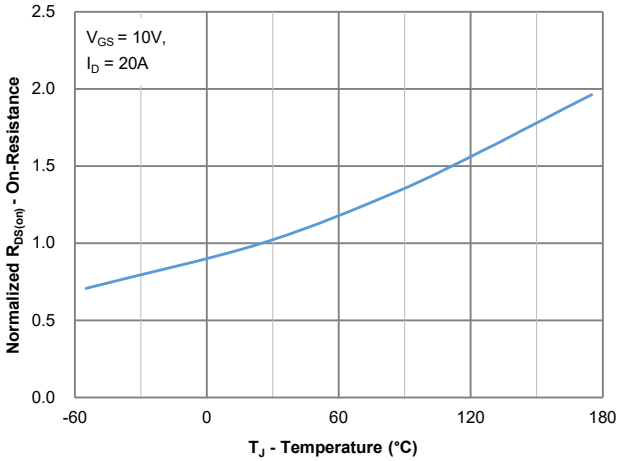


Figure 5: On-Resistance vs. Junction Temperature

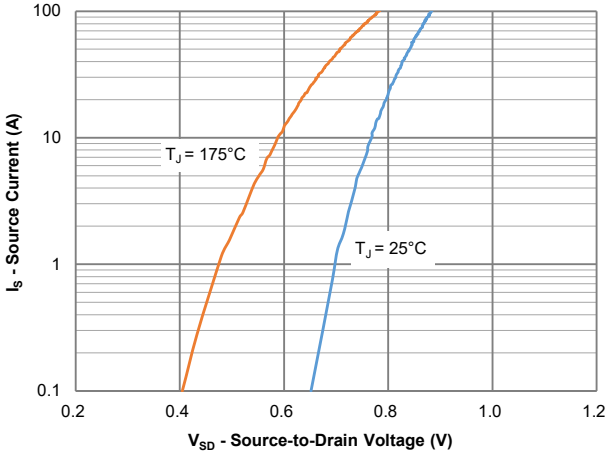


Figure 6: Source-Drain Diode Forward Voltage

Typical Electrical and Thermal Characteristics

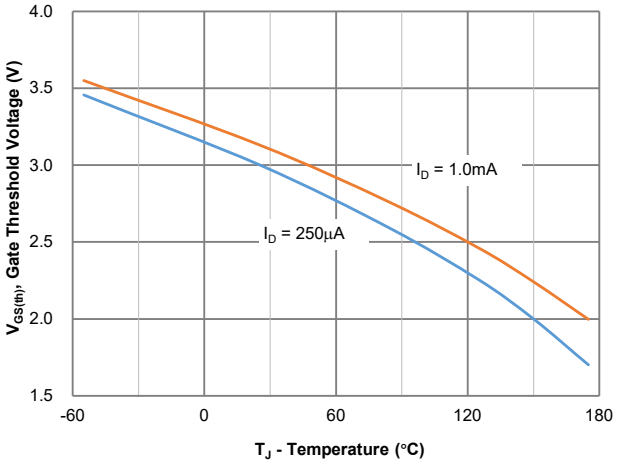


Figure 7: Gate Threshold Variation vs. Junction Temperature

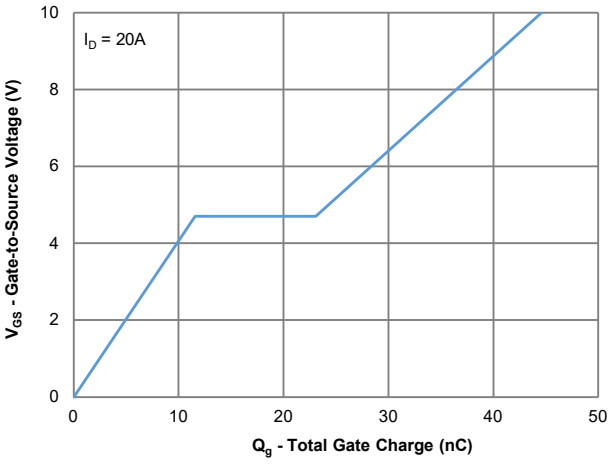


Figure 8: Gate Charge Characteristics

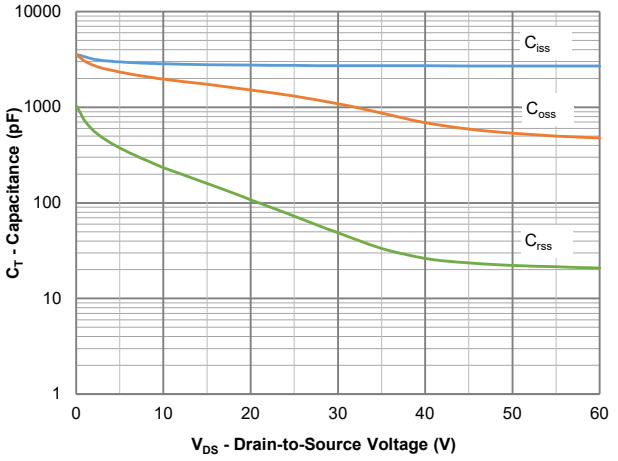


Figure 9: Capacitance Characteristics

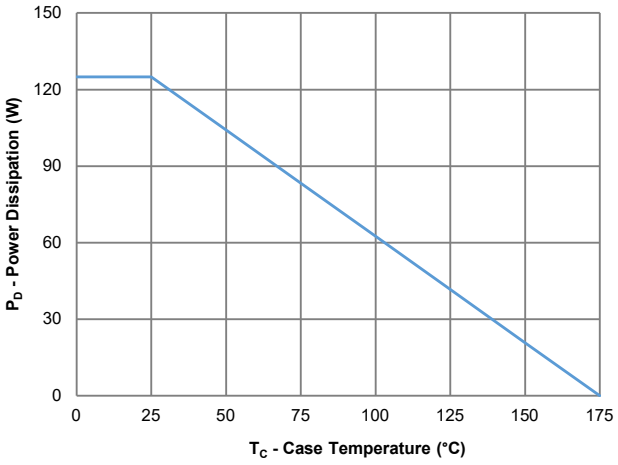


Figure 10: Power Derating

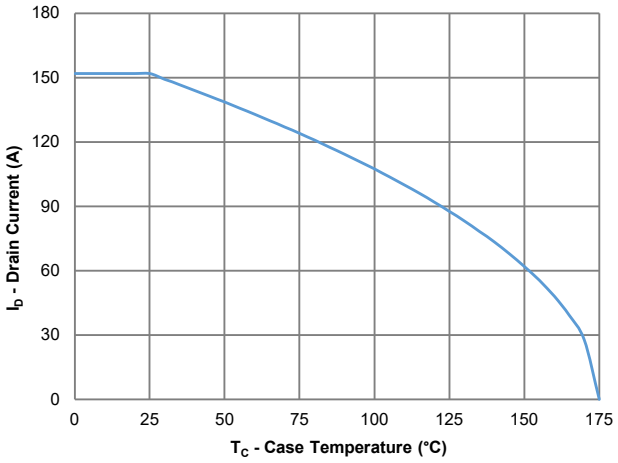


Figure 11: Current Derating

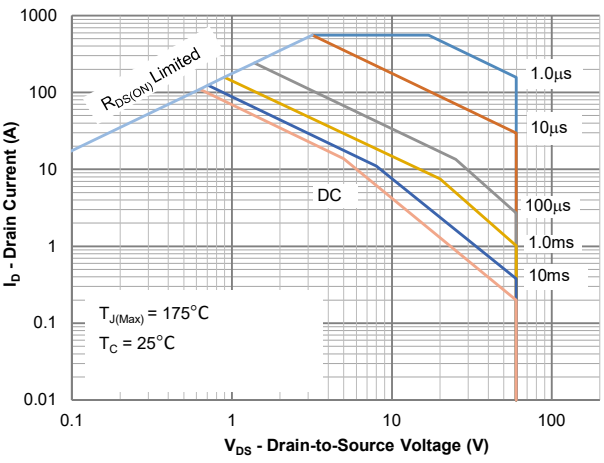


Figure 12: Safe Operating Area

Typical Electrical and Thermal Characteristics

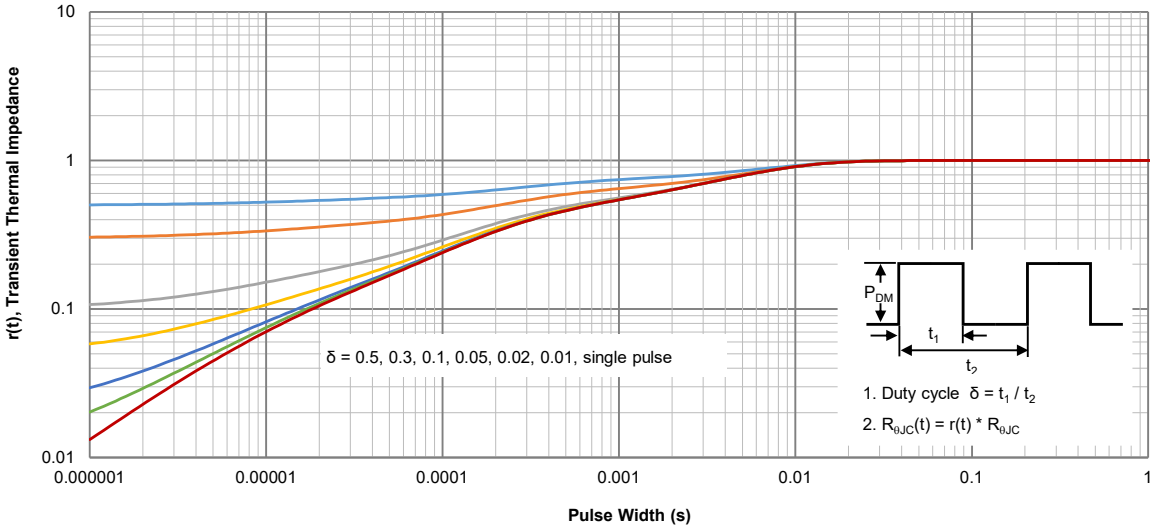
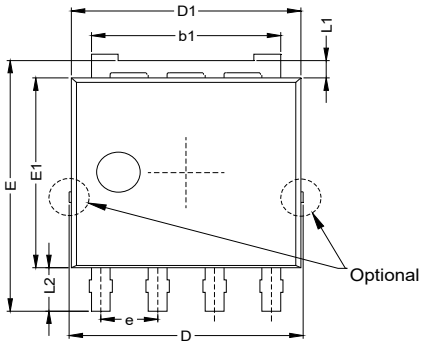


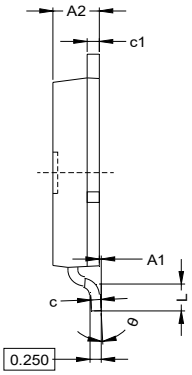
Figure 13: Normalized Maximum Transient Thermal Impedance

LFPAK5060-8L Package Outline

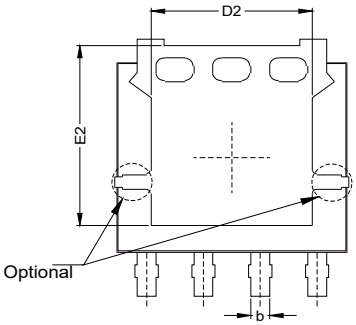
Package Outline



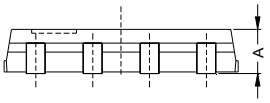
Top View



Side View



Bottom View

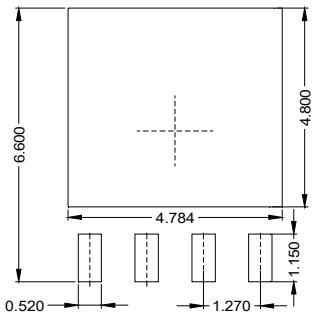


Front View

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. ALL DIMNESIONS IN MILLIMETER (ANNGLE IN DEGREE).
3. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	1.000	--	1.300
A1	0.000	--	0.150
A2	0.980	1.050	1.120
b	0.350	0.420	0.500
b1	4.020	4.230	4.410
c	0.180	0.230	0.280
c1	0.240	0.270	0.300
D	--	--	5.300
D1	4.950	5.130	5.300
D2	3.500	--	3.800
E	5.950	--	6.250
E1	4.450	4.600	4.750
E2	4.100	--	4.450
e	1.270 BSC.		
L	0.400	0.650	0.850
L1	0.270	--	0.570
L2	0.800	--	1.300
θ	0°	--	8°

Recommended Soldering Footprint



DIMENSIONS:MILLIMETERS