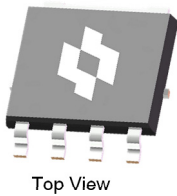
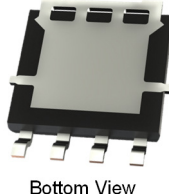
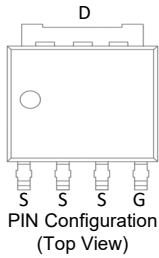
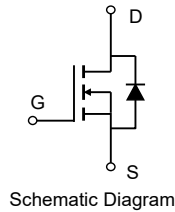


Product Summary

V_{DS}	$R_{DS(ON)_TYP}$	I_{D_MAX}
60 V	1.8 m Ω @ $V_{GS} = 10V$	168 A

LFPAK5060

Sinesemi Automotive MOSFET

Features

- N-Channel Enhancement Mode - Standard Level
- AEC-Q101 Qualified, PPAP Capable
- 175°C Operating Temperature
- 100% ΔV_{DS} & UIS & R_g Tested

Applications

- General Automotive Applications

Mechanical Data

- Green Molding Compound
- Moisture Sensitivity: Level 1 per J-STD-020
- UL Flammability Classification Rating 94V-0

Ordering Information

Orderable Part Number	Package Type	Device Marking	Form	Quantity (pcs)
SMT6002AHFP5Q	LFPAK5060	6002AHQ	13" Tape&Reel	5,000

Maximum Ratings (@ $T_C = 25^\circ\text{C}$, unless otherwise specified.)

Parameter	Symbol	Value	Unit
Drain - Source Voltage	V_{DS}	60	V
Gate - Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($V_{GS} = 10V$) ⁽¹⁾	I_D	$T_C = 25^\circ\text{C}$ 168	A
		$T_C = 100^\circ\text{C}$ 119	A
Pulsed Drain Current ⁽²⁾	I_{DM}	633	A
Single Pulse Avalanche Energy ⁽³⁾	E_{AS}	462	mJ
Single Pulse Avalanche Current ($L = 0.1\text{mH}$)	I_{AS}	54	A
Power Dissipation	P_D	$T_C = 25^\circ\text{C}$ 125	W
		$T_C = 100^\circ\text{C}$ 63	W
Junction & Storage Temperature Range	T_J, T_{STG}	-55 ~ +175	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance, Junction-to-Ambient ⁽⁴⁾	$R_{\theta JA}$	35	44	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Case ⁽⁵⁾	$R_{\theta JC}$	0.90	1.2	$^\circ\text{C/W}$

Electrical Characteristics (@ $T_J = 25^\circ\text{C}$, unless otherwise specified.)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Off Characteristics ⁽⁶⁾						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60V, V _{GS} = 0V	-	-	1.0	μA
		T _J = 125°C	-	-	100	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} = 0V	-	-	±100	nA
On Characteristics ⁽⁶⁾						
Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 250μA	2.0	3.0	4.0	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D = 20A	-	1.8	2.2	mΩ
Forward Transconductance	g _{fs}	V _{DS} = 5.0V, I _D = 20A	-	50	-	S
Diodes Forward Voltage	V _{SD}	I _S = 2.0A, V _{GS} = 0V	-	0.7	1.2	V
Dynamic Characteristics ⁽⁷⁾						
Input Capacitance	C _{iss}	V _{DS} = 30V, V _{GS} = 0V, f = 1MHz	-	3355	4362	pF
Output Capacitance	C _{oss}		-	1469	1910	pF
Reverse Transfer Capacitance	C _{rss}		-	66	132	pF
Gate Resistance	R _g	V _{GS} = 0V, V _{DS} = 0V, f = 1MHz	-	1.4	-	Ω
Switching Characteristics ⁽⁷⁾						
Turn-On DelayTime	t _{d(on)}	V _{GS} = 10V, V _{DS} = 30V I _D = 20A, R _{GEN} = 3.0Ω	-	16	-	ns
Rise Time	t _r		-	39	-	ns
Turn-Off DelayTime	t _{d(off)}		-	52	-	ns
Fall Time	t _f		-	20	-	ns
Gate Charge Characteristics ⁽⁷⁾						
Total Gate Charge (V _{GS} = 10V)	Q _g	V _{DS} = 30V, I _D = 20A V _{GS} = 10V	-	59	77	nC
Total Gate Charge (V _{GS} = 6.0V)	Q _g		-	37	48	nC
Gate-Source Charge	Q _{gs}		-	16.2	24	nC
Gate-Drain Charge	Q _{gd}		-	14.0	21	nC
Gate Plateau Voltage	V _{plateau}		-	4.7	-	V
Drain-Source Diode Characteristics ⁽⁷⁾						
Body Diode Reverse Recovery Time	t _{rr}	I _F = 20A, dI/dt = 100A/μs, T _J = 25°C	-	119	-	ns
Body Diode Reverse Recovery Charge	Q _{rr}		-	76	-	nC
Diode Forward Current	I _S	T _C = 25°C	-	-	168	A

Notes:

1. This current is chip limited, which is calculated based on R_{thjc} .
2. This current is calculated on single pulse with 10 μs Single Pulse.
3. Defined by design, not subject to production test, E_{AS} condition: $T_J = 25^\circ\text{C}$, $V_{DD} = 30V$, $V_{GS} = 10V$, $L = 1.0\text{mH}$.
4. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
5. Thermal resistance from junction to the exposed drain pad.
6. Short duration pulse test used to minimize self-heating effect.
7. Defined by design, not subject to production.

Typical Electrical and Thermal Characteristics

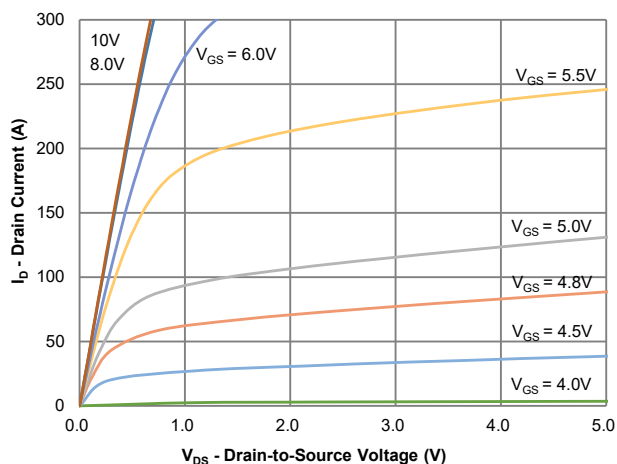


Figure 1: Output Characteristics

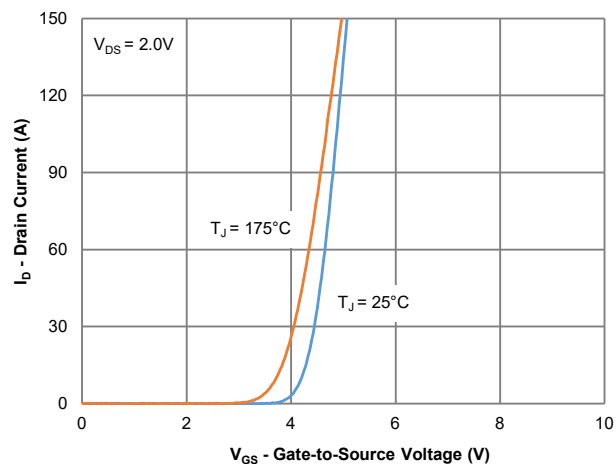


Figure 2: Transfer Characteristics

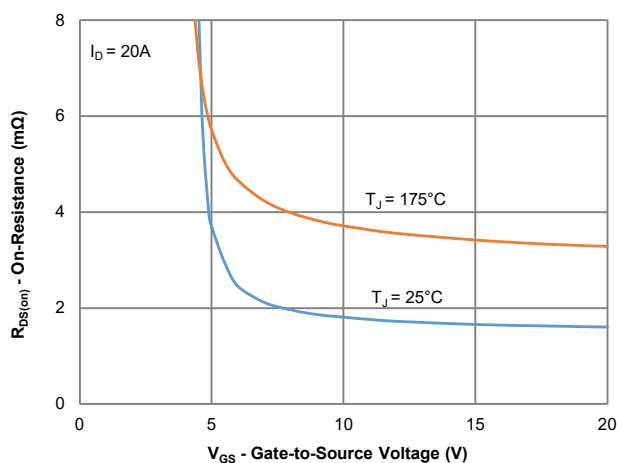


Figure 3: On-Resistance vs. Gate-Source Voltage

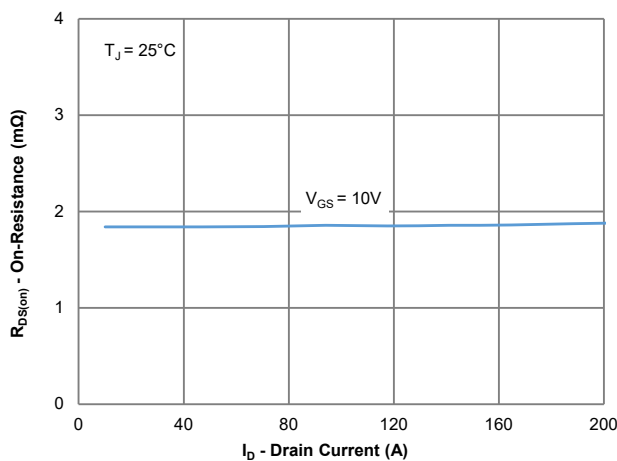


Figure 4: On-Resistance vs. Drain Current and Gate Voltage

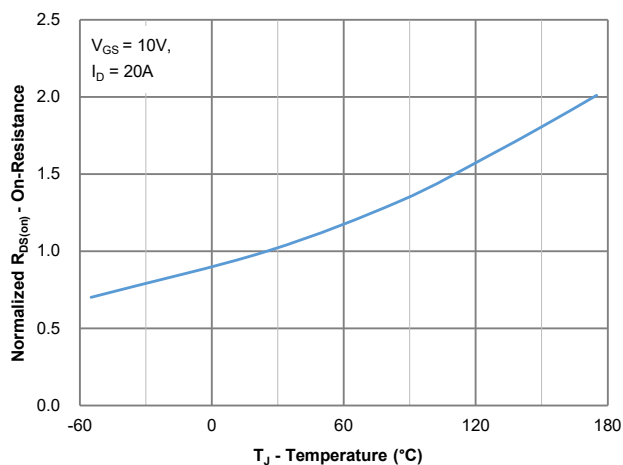


Figure 5: On-Resistance vs. Junction Temperature

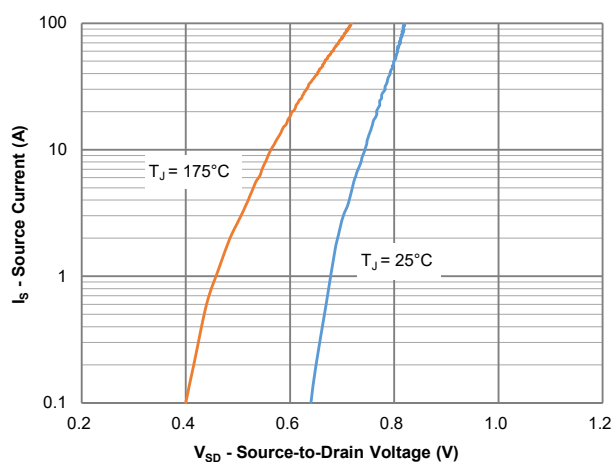


Figure 6: Source-Drain Diode Forward Voltage

Typical Electrical and Thermal Characteristics

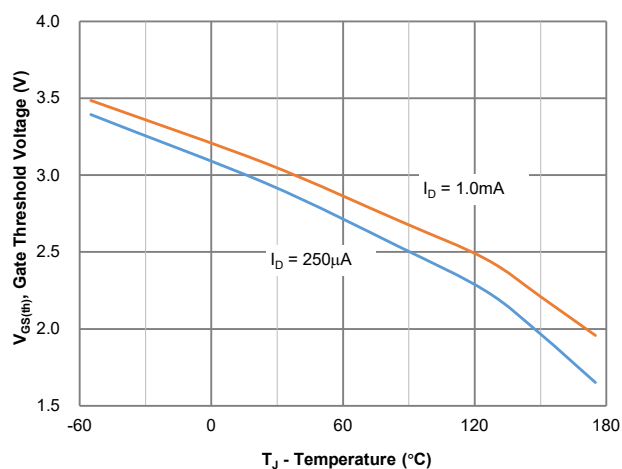


Figure 7: Gate Threshold Variation vs. Junction Temperature

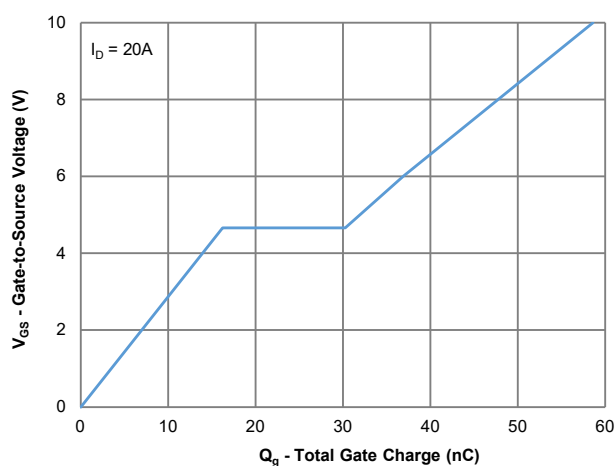


Figure 8: Gate Charge Characteristics

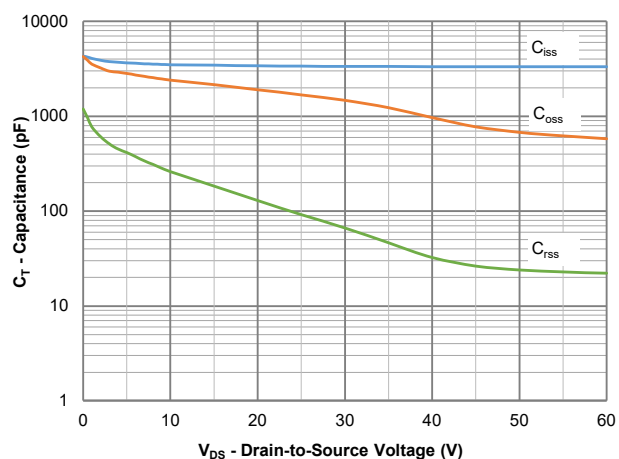


Figure 9: Capacitance Characteristics

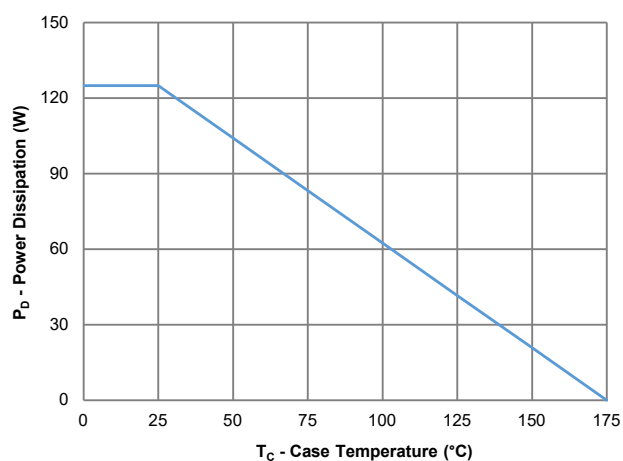


Figure 10: Power Derating

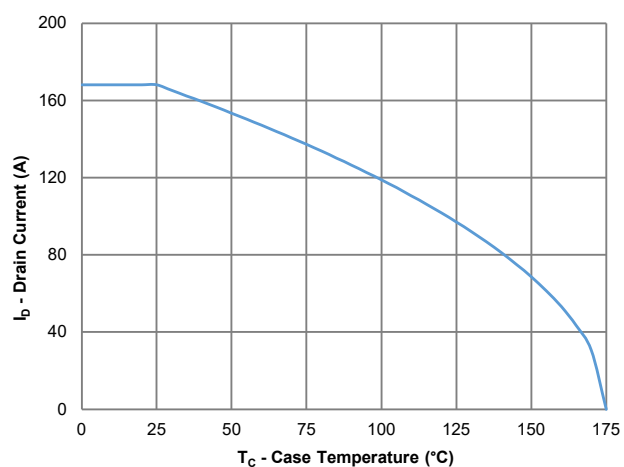


Figure 11: Current Derating

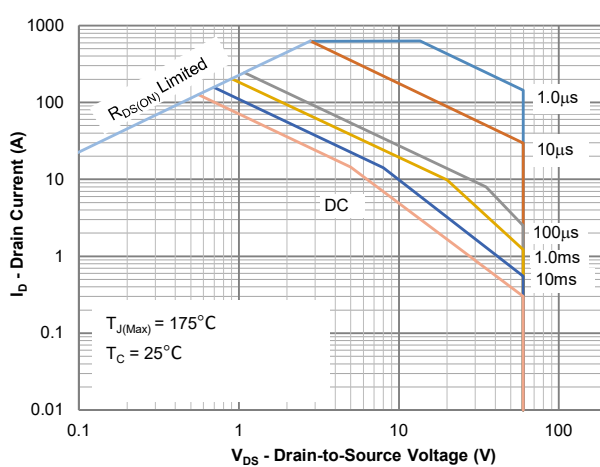
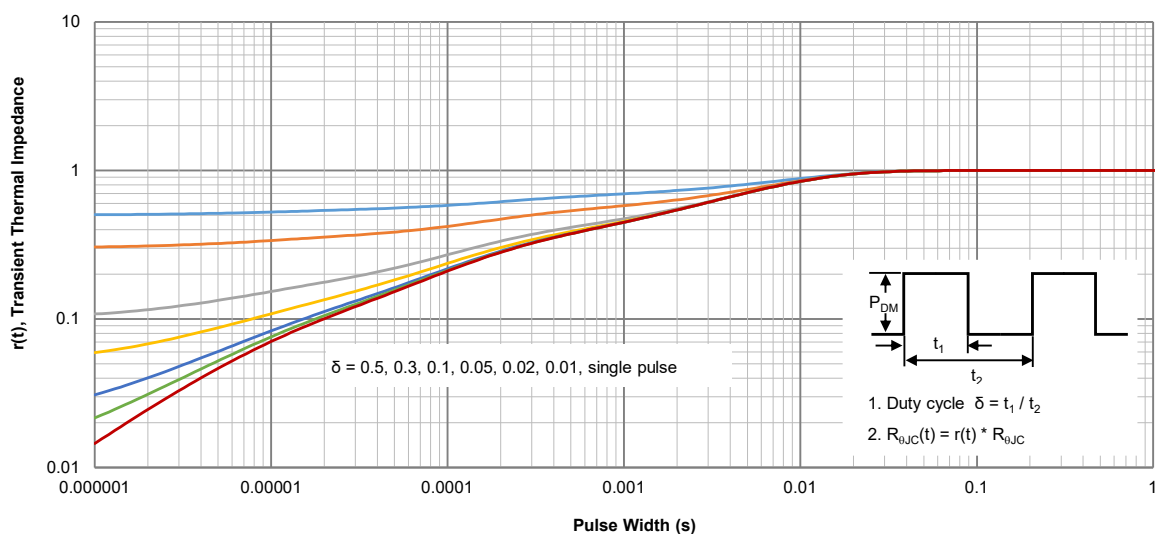
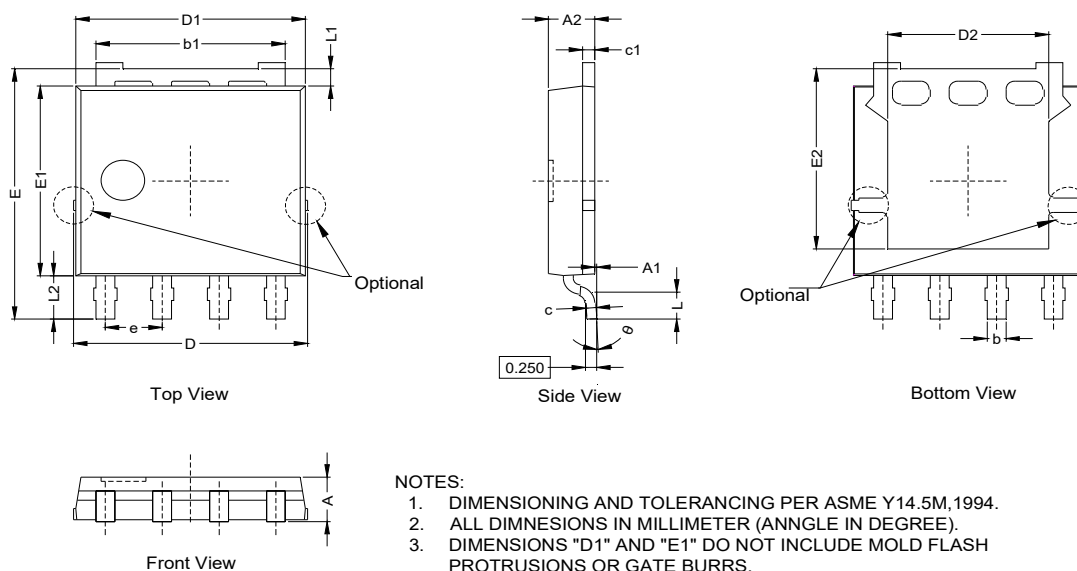
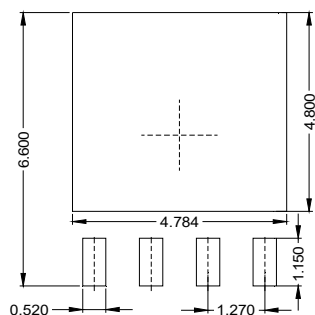


Figure 12: Safe Operating Area

Typical Electrical and Thermal Characteristics

Figure 13: Normalized Maximum Transient Thermal Impedance

LFP5060 Package Outline
Package Outline


DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	1.000	--	1.300
A1	0.000	--	0.150
A2	0.980	1.050	1.120
b	0.350	0.420	0.500
b1	4.020	4.230	4.410
c	0.180	0.230	0.280
c1	0.240	0.270	0.300
D	--	--	5.300
D1	4.950	5.130	5.300
D2	3.500	--	3.800
E	5.950	--	6.250
E1	4.450	4.600	4.750
E2	4.100	--	4.450
e	1.270 BSC.		
L	0.400	0.650	0.850
L1	0.270	--	0.570
L2	0.800	--	1.300
θ	0°	--	8°

Recommended Soldering Footprint


DIMENSIONS:MILLIMETERS