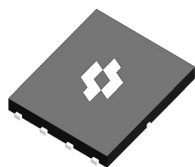
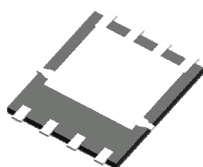


Product Summary

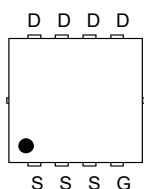
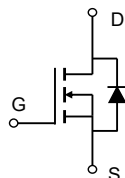
V_{DS}	$R_{DS(ON)_TYP}$	I_{D_MAX}
40 V	0.70 mΩ @ $V_{GS} = 10V$	318 A

PDFN5060-8L


Top View



Bottom View


 PIN Configuration
(Top View)


Schematic Diagram

Features

- Low On-Resistance
- Excellent FoM (figure of merit)
- 100% ΔVDS & UIS & Rg tested


Applications

- Load switching
- Motor drives
- High frequency switching, synchronous rectification

Mechanical Data

- Green molding compound
- Moisture sensitivity: level 1 per J-STD-020
- UL flammability classification rating 94V-0

Ordering Information

Orderable Part Number	Package Type	Device Marking	Form	Quantity (pcs)
SMT400SAHP	PDFN5060-8L	400SAH	13" Tape&Reel	5,000

Maximum Ratings (@ $T_C = 25^\circ\text{C}$, unless otherwise specified.)

Parameter	Symbol	Value	Unit
Drain - Source Voltage	V_{DS}	40	V
Gate - Source Voltage	V_{GS}	±20	V
Continuous Drain Current ($V_{GS} = 10V$) ⁽¹⁾	I_D	318	A
		201	A
Pulsed Drain Current ⁽²⁾	I_{DM}	1274	A
Single Pulse Avalanche Energy ⁽³⁾	E_{AS}	1040	mJ
Single Pulse Avalanche Current ($L = 0.3mH$)	I_{AS}	55	A
Power Dissipation	P_D	132	W
		53	W
Junction & Storage Temperature Range	T_J, T_{STG}	-55 ~ +150	°C

Thermal Characteristics

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance, Junction-to-Ambient ⁽⁴⁾	$R_{\theta JA}$	32	40	°C/W
Thermal Resistance, Junction-to-Case ⁽⁵⁾	$R_{\theta JC}$	0.73	0.95	°C/W

Electrical Characteristics (@ $T_J = 25^\circ\text{C}$, unless otherwise specified.)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Off Characteristics ⁽⁶⁾						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	40	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 40V, V _{GS} = 0V	-	-	1.0	μA
		T _J = 125°C	-	-	100	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} = 0V	-	-	±100	nA
On Characteristics ⁽⁶⁾						
Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 250μA	2.0	3.0	4.0	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D = 20A	-	0.70	0.85	mΩ
Forward Transconductance	g _{fs}	V _{DS} = 5.0V, I _D = 20A	-	66	-	S
Diodes Forward Voltage	V _{SD}	I _S = 2.0A, V _{GS} = 0V	-	0.7	1.2	V
Dynamic Characteristics ⁽⁷⁾						
Input Capacitance	C _{iss}	V _{DS} = 20V, V _{GS} = 0V, f = 1MHz	-	5271	-	pF
Output Capacitance	C _{oss}		-	2951	-	pF
Reverse Transfer Capacitance	C _{rss}		-	78	-	pF
Gate Resistance	R _g	V _{GS} = 0V, V _{DS} = 0V, f = 1MHz	-	1.4	-	Ω
Switching Characteristics ⁽⁷⁾						
Turn-On DelayTime	t _{d(on)}	V _{GS} = 10V, V _{DS} = 20V I _D = 20A, R _{GEN} = 3.0Ω	-	9.0	-	ns
Rise Time	t _r		-	18	-	ns
Turn-Off DelayTime	t _{d(off)}		-	40	-	ns
Fall Time	t _f		-	18	-	ns
Gate Charge Characteristics ⁽⁷⁾						
Total Gate Charge (V _{GS} = 10V)	Q _g	V _{DS} = 20V, I _D = 20A V _{GS} = 10V	-	71	-	nC
Total Gate Charge (V _{GS} = 7.0V)	Q _g		-	51	-	nC
Gate-Source Charge	Q _{gs}		-	21	-	nC
Gate-Drain Charge	Q _{gd}		-	12.9	-	nC
Gate Plateau Voltage	V _{plateau}		-	4.4	-	V
Drain-Source Diode Characteristics ⁽⁷⁾						
Body Diode Reverse Recovery Time	t _{rr}	I _F = 20A, dI/dt = 100A/μs, T _J = 25°C	-	63	-	ns
Body Diode Reverse Recovery Charge	Q _{rr}		-	92	-	nC
Diode Forward Current	I _S	T _C = 25°C	-	-	318	A

Notes:

1. This current is chip limited, which is calculated based on R_{thjc} .
2. This current is calculated on single pulse with 10 μs Single Pulse.
3. Defined by design, not subject to production test, E_{AS} condition: $T_J = 25^\circ\text{C}$, $V_{DD} = 20V$, $V_{GS} = 10V$, $L = 1.0\text{mH}$.
4. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
5. Thermal resistance from junction to the exposed pad.
6. Short duration pulse test used to minimize self-heating effect.
7. Defined by design, not subject to production.

Typical Electrical and Thermal Characteristics

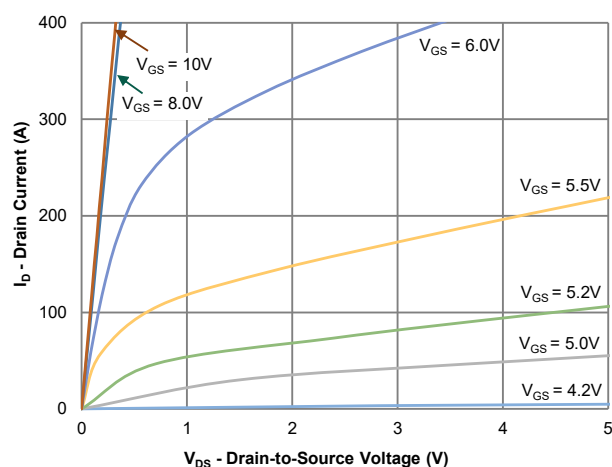


Figure 1: Output Characteristics

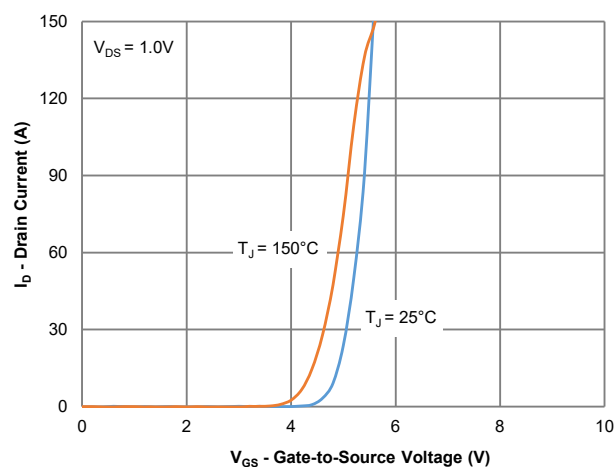


Figure 2: Transfer Characteristics

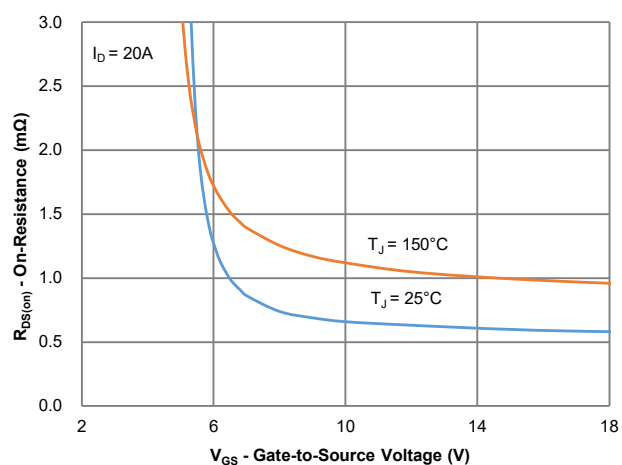


Figure 3: On-Resistance vs. Gate-Source Voltage

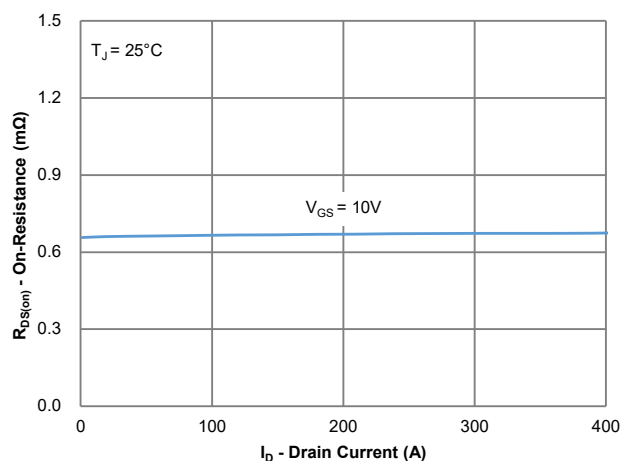


Figure 4: On-Resistance vs. Drain Current and Gate Voltage

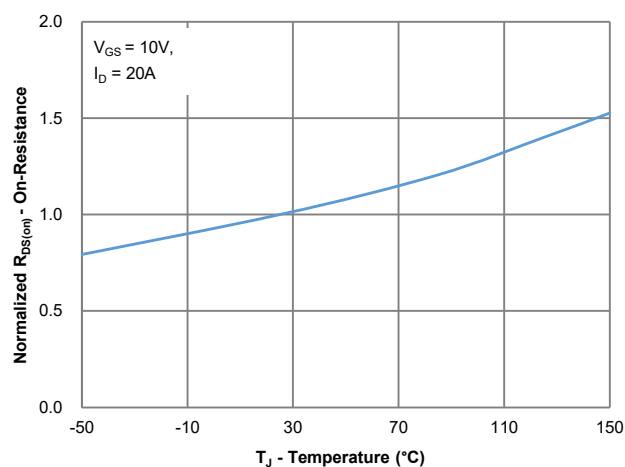


Figure 5: On-Resistance vs. Junction Temperature

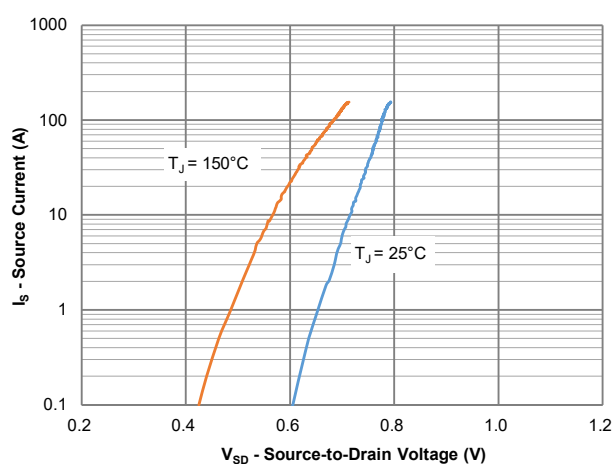


Figure 6: Source-Drain Diode Forward Voltage

Typical Electrical and Thermal Characteristics

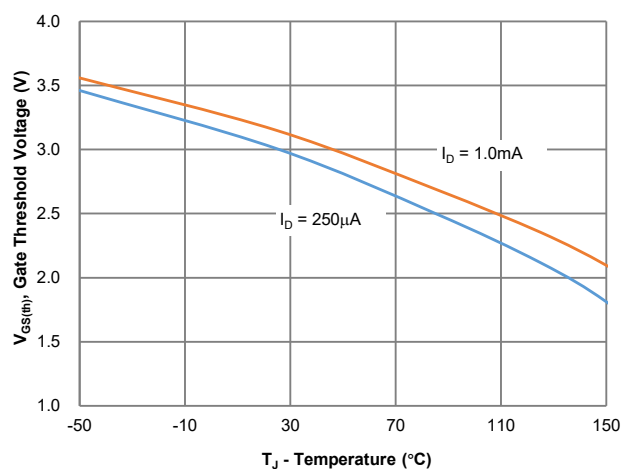


Figure 7: Gate Threshold Variation vs. Junction Temperature

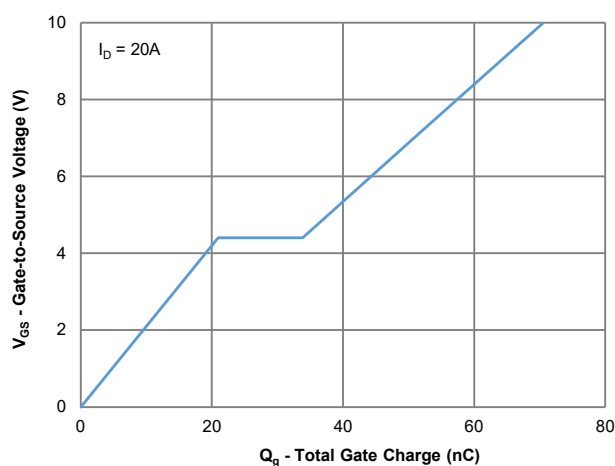


Figure 8: Gate Charge Characteristics

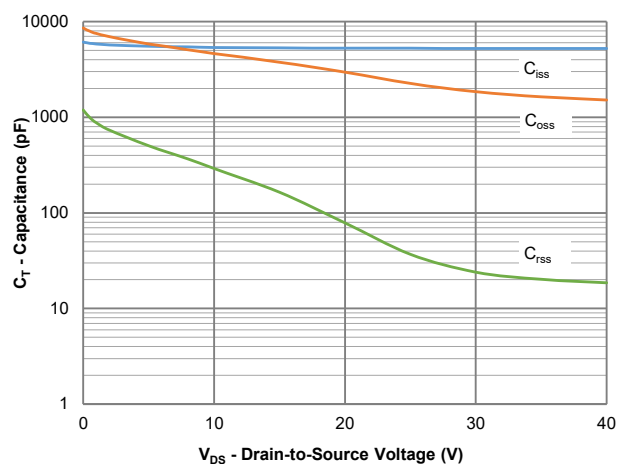


Figure 9: Capacitance Characteristics

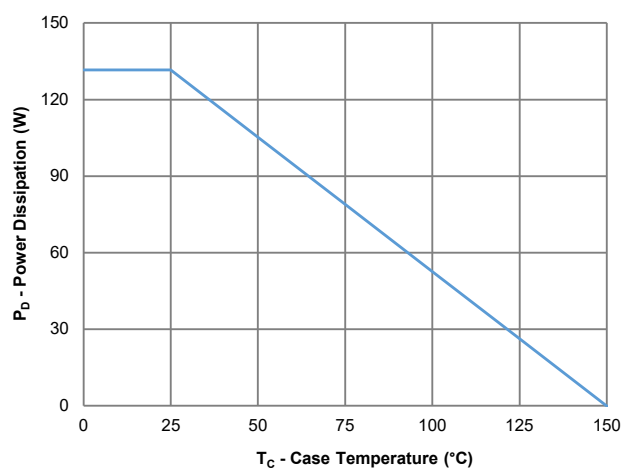


Figure 10: Power Derating

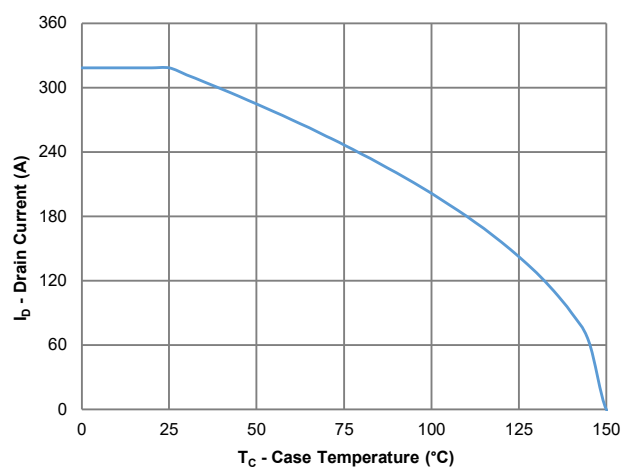


Figure 11: Current Derating

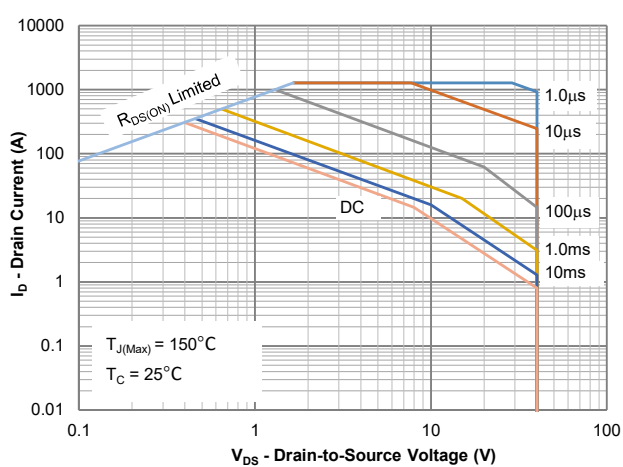
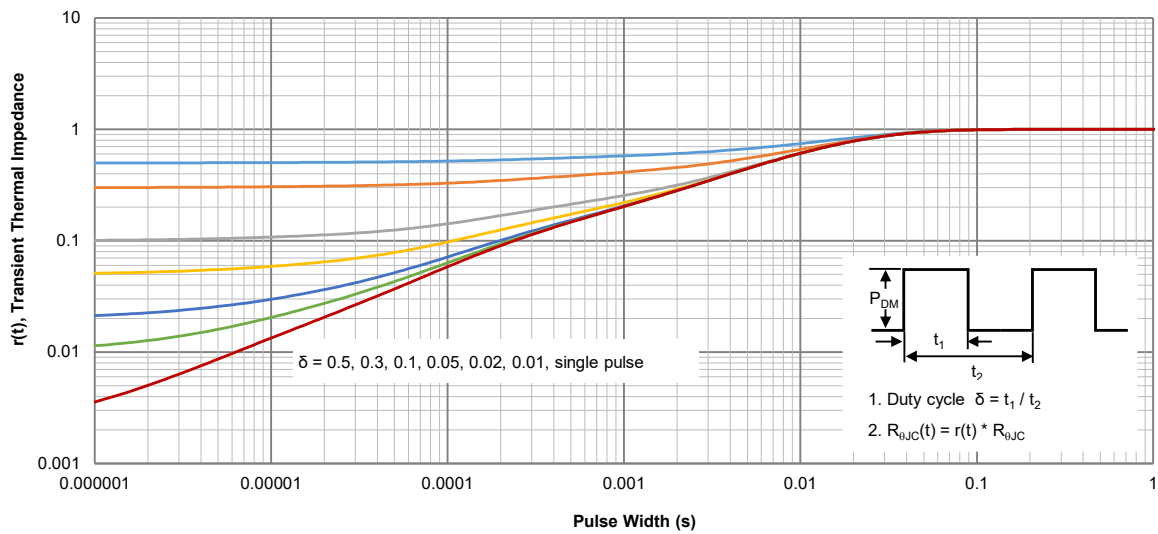
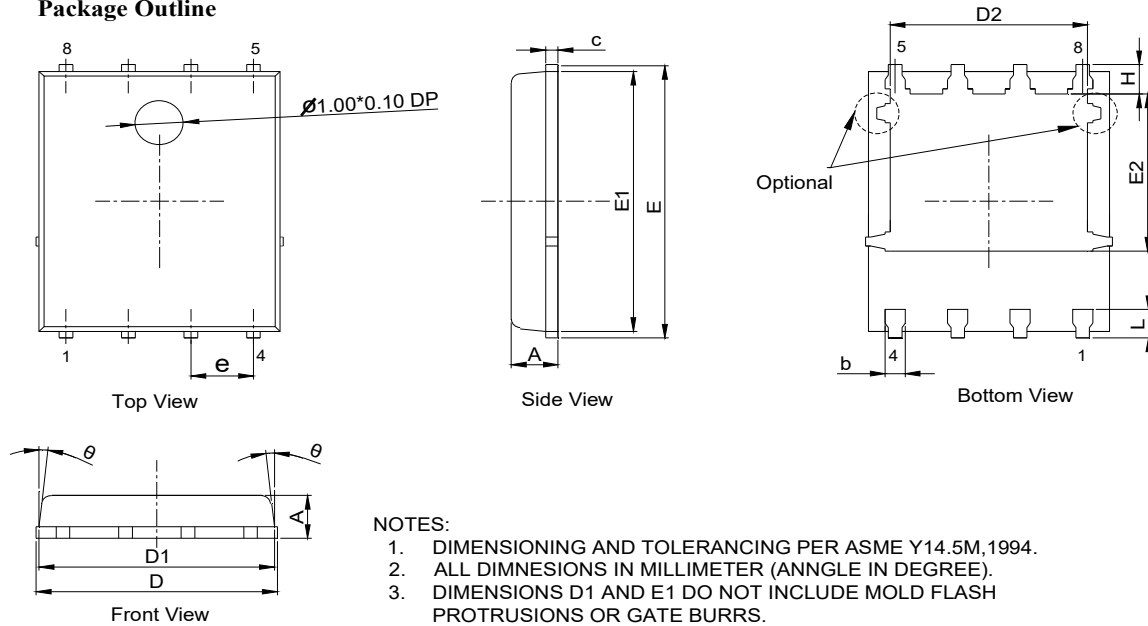
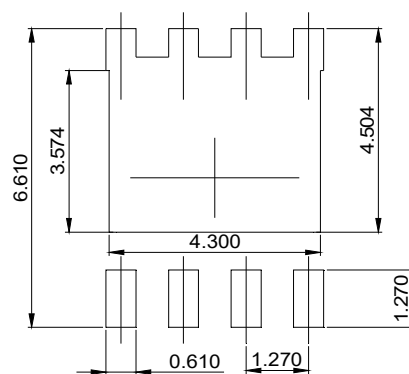


Figure 12: Safe Operating Area

Typical Electrical and Thermal Characteristics

Figure 13: Normalized Maximum Transient Thermal Impedance

PDFN5060-8L Package Outline
Package Outline


DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
b	0.20	—	0.51
c	0.21	0.25	0.34
D	4.90	—	5.40
D1	4.80	—	5.15
D2	3.70	—	4.20
E	5.90	—	6.50
E1	5.65	5.80	5.95
E2	3.32	3.50	3.63
e	1.27BSC		
H	0.50	—	0.93
L	0.45	—	0.91
θ	0°	—	12°

Recommended Soldering Footprint


DIMENSIONS: MILLIMETERS