

Product Summary

V_{DS}	$R_{DS(ON_MAX)}$	I_{D_MAX}
100 V	20 m Ω @ $V_{GS} = 10V$	32 A
	27 m Ω @ $V_{GS} = 4.5V$	

Sinesemi Automotive MOSFET

Features

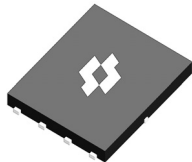
- N-Channel Enhancement Mode - Logic Level
- AEC-Q101 Qualified, PPAP Capable
- 175°C Operating Temperature
- 100% UIS and R_g Tested

Applications

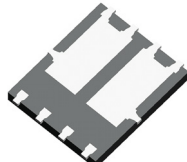
- General Automotive Applications

Mechanical Data

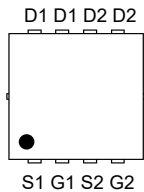
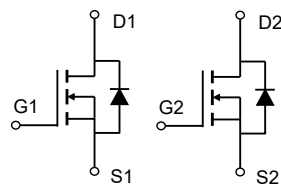
- Green Molding Compound
- Moisture Sensitivity: Level 1 per J-STD-020
- UL Flammability Classification Rating 94V-0

PDFN5060-8L-D


Top View



Bottom View


 PIN Configuration
(Top View)

 Chip-1 & Chip-2
Schematic Diagram

Ordering Information

Orderable Part Number	Package Type	Device Marking	Form	Quantity (pcs)
SMT10T20ALPDQ	PDFN5060-8L-D	10T20ALDQ	13" Tape&Reel	5,000

Maximum Ratings (@ $T_C = 25^\circ\text{C}$, unless otherwise specified.)

Parameter	Symbol	Value	Unit
Drain - Source Voltage	V_{DS}	100	V
Gate - Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($V_{GS} = 10V$) ⁽¹⁾	I_D	32	A
		23	A
Pulsed Drain Current ⁽²⁾	I_{DM}	125	A
Single Pulse Avalanche Energy ⁽³⁾	E_{AS}	40	mJ
Single Pulse Avalanche Current ($L = 0.1\text{mH}$)	I_{AS}	16	A
Power Dissipation	P_D	43	W
		21	W
Junction & Storage Temperature Range	T_J, T_{STG}	-55 ~ +175	$^\circ\text{C}$

Thermal Characteristics

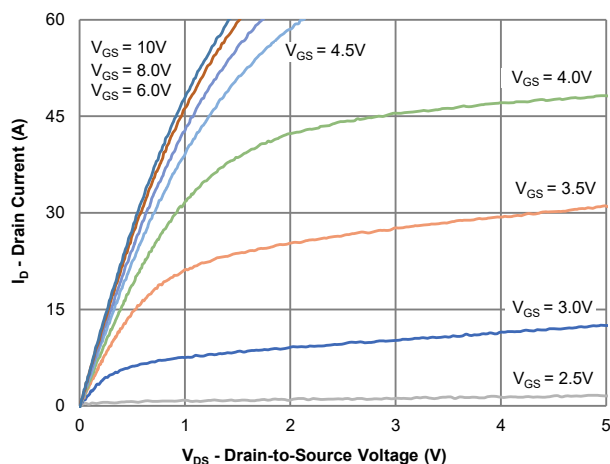
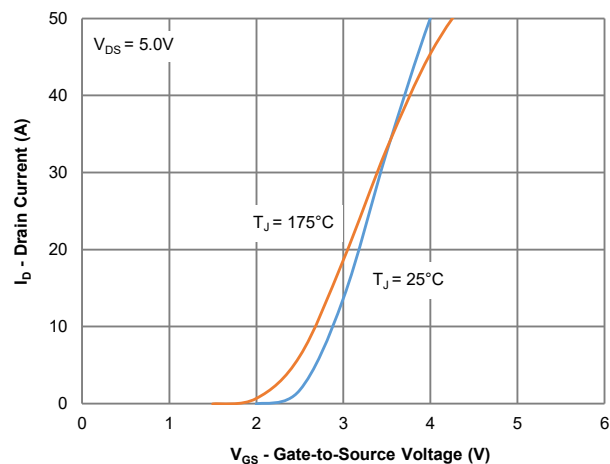
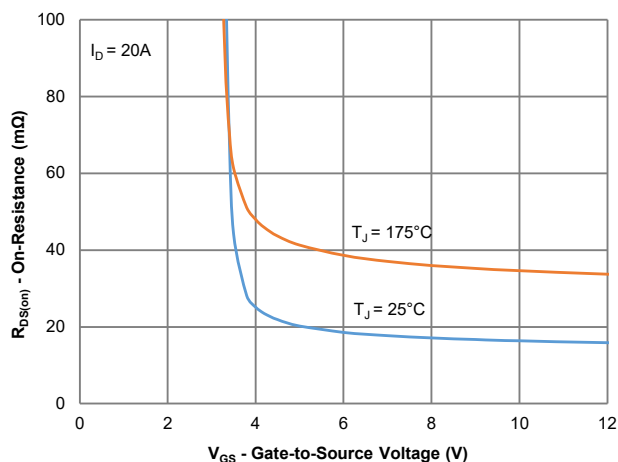
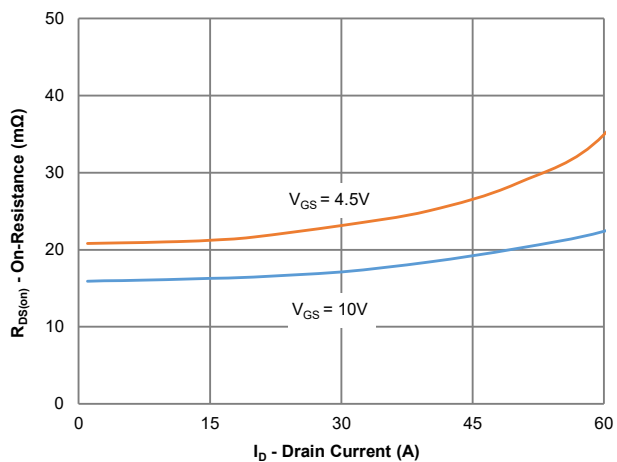
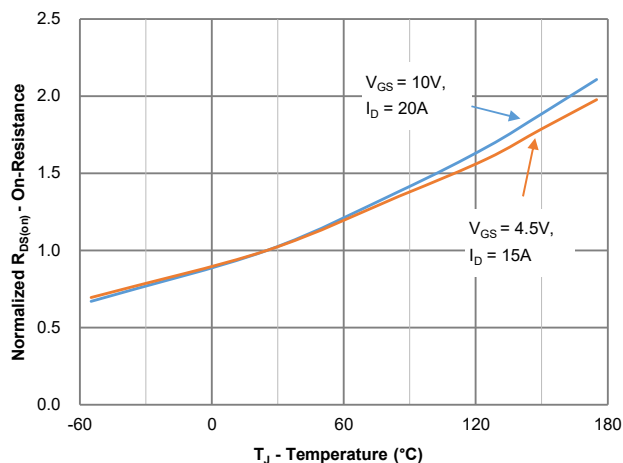
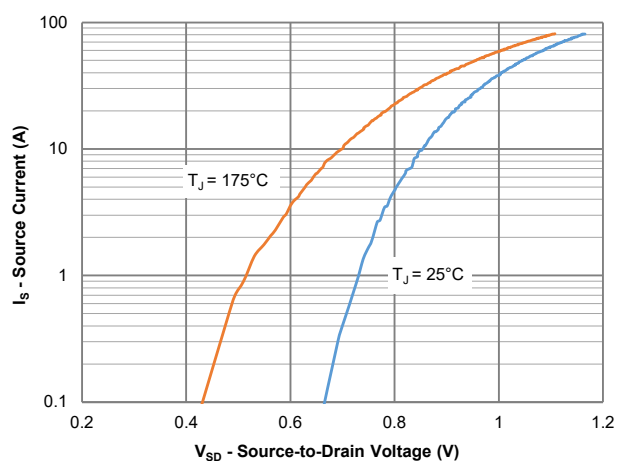
Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance, Junction-to-Ambient ⁽⁴⁾	$R_{\theta JA}$	45	56	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Case ⁽⁵⁾	$R_{\theta JC}$	2.7	3.5	$^\circ\text{C/W}$

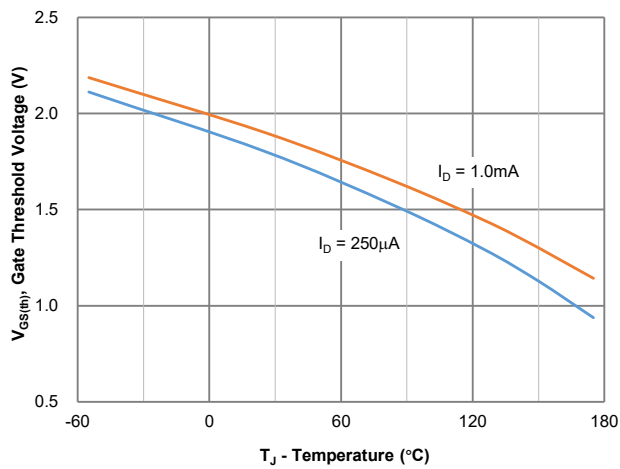
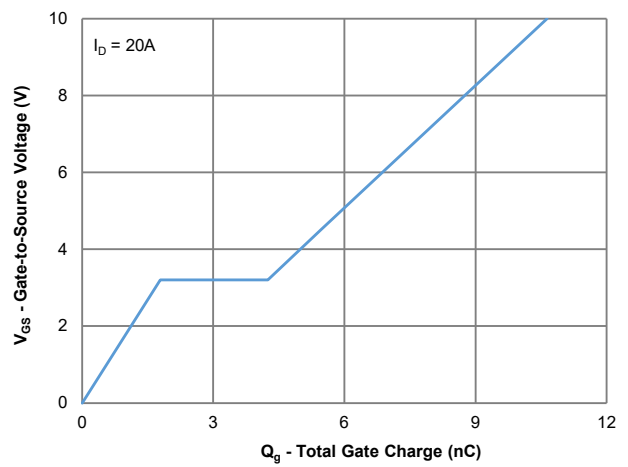
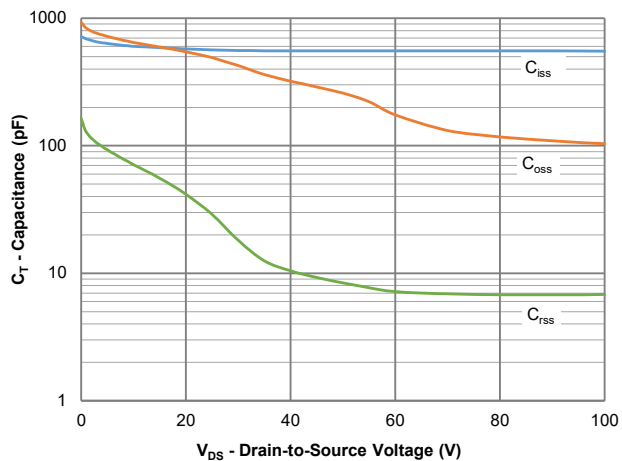
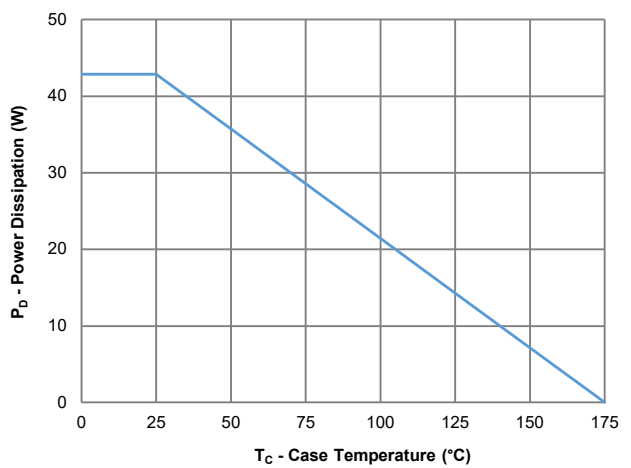
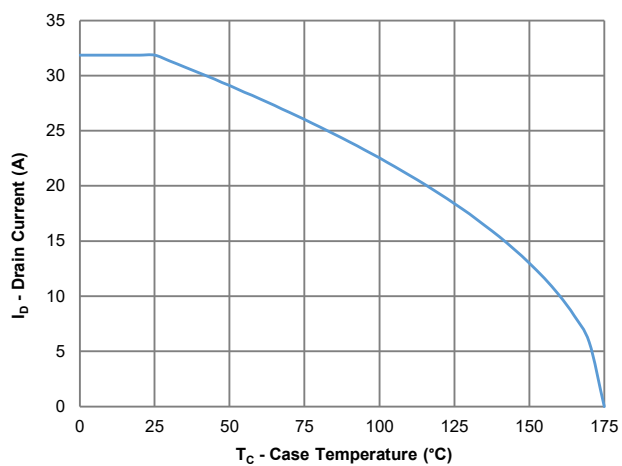
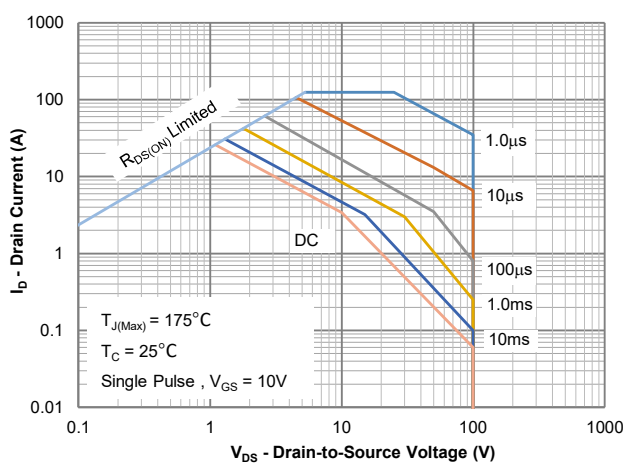
Electrical Characteristics(Chip-1 & Chip-2) (@ $T_J = 25^\circ\text{C}$, unless otherwise specified.)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Off Characteristics ⁽⁶⁾						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100V, V _{GS} = 0V	-	-	1.0	μA
		T _J = 125°C	-	-	100	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} = 0V	-	-	±100	nA
On Characteristics ⁽⁶⁾						
Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 250μA	1.2	1.8	2.5	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D = 20A	-	16.5	20	mΩ
		V _{GS} = 4.5V, I _D = 15A	-	21	27	mΩ
Forward Transconductance	g _{fs}	V _{DS} = 5.0V, I _D = 20A	-	20	-	S
Diodes Forward Voltage	V _{SD}	I _S = 2.0A, V _{GS} = 0V	-	0.7	1.2	V
Dynamic Characteristics ⁽⁷⁾						
Input Capacitance	C _{iss}	V _{DS} = 50V, V _{GS} = 0V, f = 1MHz	-	554	720	pF
Output Capacitance	C _{oss}		-	258	335	pF
Reverse Transfer Capacitance	C _{rss}		-	8.4	17	pF
Gate Resistance	R _g	V _{GS} = 0V, V _{DS} = 0V, f = 1MHz	-	1.0	-	Ω
Switching Characteristics ⁽⁷⁾						
Turn-On DelayTime	t _{d(on)}	V _{GS} = 10V, V _{DS} = 50V I _D = 20A, R _{GEN} = 3.0Ω	-	3.2	-	ns
Rise Time	t _r		-	2.7	-	ns
Turn-Off DelayTime	t _{d(off)}		-	10.5	-	ns
Fall Time	t _f		-	4.0	-	ns
Gate Charge Characteristics ⁽⁷⁾						
Total Gate Charge (V _{GS} = 10V)	Q _g	V _{DS} = 50V, I _D = 20A V _{GS} = 10V	-	10.6	13.8	nC
Total Gate Charge (V _{GS} = 4.5V)	Q _g		-	5.5	7.2	nC
Gate-Source Charge	Q _{gs}		-	1.8	2.7	nC
Gate-Drain Charge	Q _{gd}		-	2.5	3.8	nC
Gate Plateau Voltage	V _{plateau}		-	3.2	-	V
Drain-Source Diode Characteristics ⁽⁷⁾						
Body Diode Reverse Recovery Time	t _{rr}	I _F = 20A, dI/dt = 100A/μs, T _J = 25°C	-	34	-	ns
Body Diode Reverse Recovery Charge	Q _{rr}		-	39	-	nC
Diode Forward Current	I _S	T _C = 25°C	-	-	32	A

Notes:

1. This current is chip limited, which is calculated based on R_{thjc} .
2. This current is calculated on single pulse with 10 μs Pulse & Duty Cycle = 1%.
3. Defined by design, not subject to production test, E_{AS} condition: $T_J=25^\circ\text{C}, V_{DD}=50V, V_{GS}=10V, L=1.0\text{mH}$.
4. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
5. Thermal resistance from junction to soldering point (on the exposed drain pad).
6. Short duration pulse test used to minimize self-heating effect.
7. Defined by design, not subject to production.

Typical Electrical and Thermal Characteristics(Chip-1 & Chip-2)

Figure 1: Output Characteristics

Figure 2: Transfer Characteristics

Figure 3: On-Resistance vs. Gate-Source Voltage

Figure 4: On-Resistance vs. Gate-Source Voltage

Figure 5: On-Resistance vs. Junction Temperature

Figure 6: Source-Drain Diode Forward Voltage

Typical Electrical and Thermal Characteristics(Chip-1 & Chip-2)

Figure 7: Gate Threshold Variation vs. Junction Temperature

Figure 8: Gate Charge Characteristics

Figure 9: Capacitance Characteristics

Figure 10: Power Derating

Figure 11: Current Derating

Figure 12: Safe Operating Area

Typical Electrical and Thermal Characteristics(Chip-1 & Chip-2)

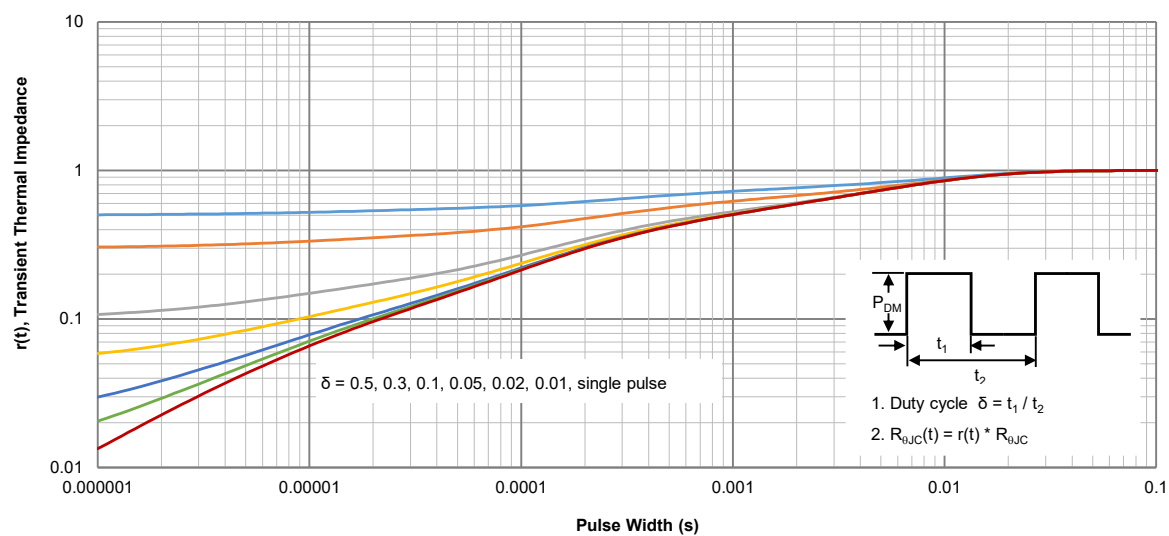
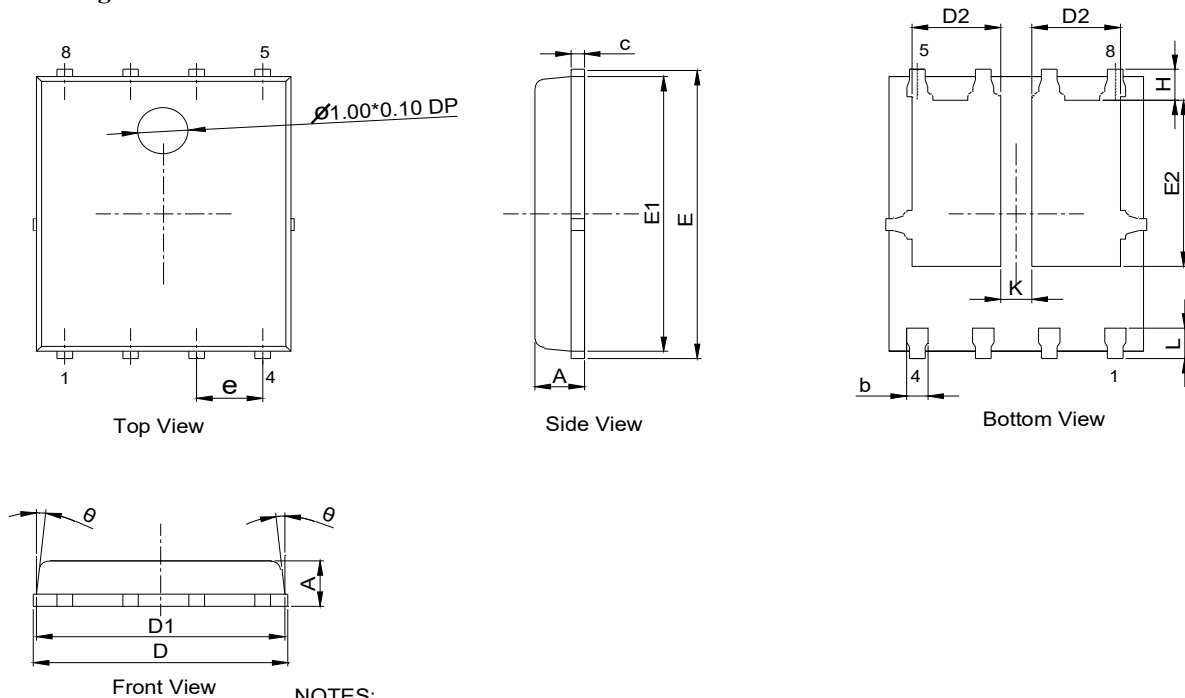


Figure 13: Normalized Maximum Transient Thermal Impedance

PDFN5060-8L-D Package Outline

Package Outline

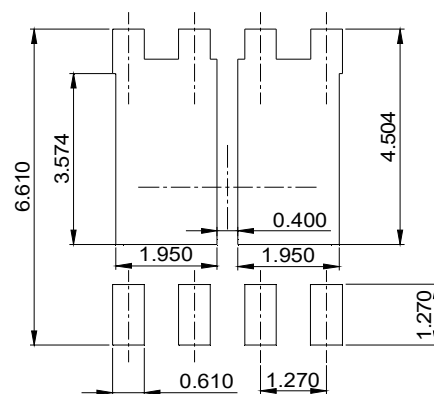


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. ALL DIMENSIONS IN MILLIMETER (ANGLE IN DEGREE).
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
b	0.20	--	0.51
c	0.21	0.25	0.34
D	4.85	5.00	5.15
D1	4.80	4.90	5.00
D2	1.50	--	1.80
E	5.90	6.00	6.10
E1	5.65	5.75	5.85
E2	3.38	3.48	3.78
e	1.27BSC		
H	0.41	--	0.75
L	0.45	0.60	0.75
K	0.60 REF		
θ	0°	--	12°

Recommended Soldering Footprint



DIMENSIONS:MILLIMETERS