

Product Summary

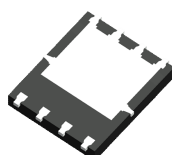
V_{DS}	$R_{DS(ON)_TYP}$	I_{D_MAX}
100 V	7.7 m Ω @ $V_{GS} = 10V$	67 A
	9.9 m Ω @ $V_{GS} = 4.5V$	

Features

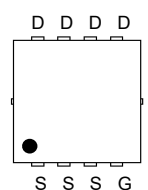
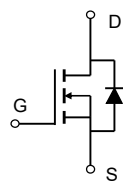
- Low On-Resistance
- Excellent FoM (figure of merit)
- 100% ΔV_{DS} & UIS & Rg Tested

PDFN5060-8L


Top View



Bottom View


 PIN Configuration
(Top View)


Schematic Diagram


Applications

- Motor controls
- DC/DC in Telecoms and Industrial
- High frequency switching, synchronous rectification

Mechanical Data

- Green Molding Compound
- Moisture Sensitivity: Level 1 per J-STD-020
- UL Flammability Classification Rating 94V-0

Ordering Information

Orderable Part Number	Package Type	Device Marking	Form	Quantity (pcs)
SMT10T09ALPX	PDFN5060-8L	10T09ALX	13" Tape&Reel	5,000

Maximum Ratings (@ $T_C = 25^\circ\text{C}$, unless otherwise specified.)

Parameter	Symbol	Value	Unit
Drain - Source Voltage	V_{DS}	100	V
Gate - Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($V_{GS} = 10V$) ⁽¹⁾	I_D	67	A
		42	A
Pulsed Drain Current ⁽²⁾	I_{DM}	246	A
Single Pulse Avalanche Energy ⁽³⁾	E_{AS}	130	mJ
Single Pulse Avalanche Current ($L = 0.1\text{mH}$)	I_{AS}	30	A
Power Dissipation	P_D	74	W
		29	W
Junction & Storage Temperature Range	T_J, T_{STG}	-55 ~ +150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance, Junction-to-Ambient ⁽⁴⁾	$R_{\theta JA}$	37	46	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Case ⁽⁵⁾	$R_{\theta JC}$	1.3	1.7	$^\circ\text{C/W}$

Electrical Characteristics (@ $T_J = 25^\circ\text{C}$, unless otherwise specified.)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Off Characteristics ⁽⁶⁾						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100V, V _{GS} = 0V	-	-	1.0	μA
		T _J = 125°C	-	-	100	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} = 0V	-	-	±100	nA
On Characteristics ⁽⁶⁾						
Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 250μA	1.2	1.7	2.5	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 10V, I _D = 20A	-	7.7	9.2	mΩ
		V _{GS} = 4.5V, I _D = 15A	-	9.9	11.9	mΩ
Forward Transconductance	g _{fs}	V _{DS} = 5.0V, I _D = 20A	-	31	-	S
Diodes Forward Voltage	V _{SD}	I _S = 2.0A, V _{GS} = 0V	-	0.7	1.2	V
Dynamic Characteristics ⁽⁷⁾						
Input Capacitance	C _{iss}	V _{DS} = 50V, V _{GS} = 0V, f = 1MHz	-	1604	-	pF
Output Capacitance	C _{oss}		-	576	-	pF
Reverse Transfer Capacitance	C _{rss}		-	18	-	pF
Gate Resistance	R _g	V _{GS} = 0V, V _{DS} = 0V, f = 1MHz	-	0.9	-	Ω
Switching Characteristics ⁽⁷⁾						
Turn-On DelayTime	t _{d(on)}	V _{GS} = 10V, V _{DS} = 50V I _D = 20A, R _{GEN} = 3.0Ω	-	4.7	-	ns
Rise Time	t _r		-	10.2	-	ns
Turn-Off DelayTime	t _{d(off)}		-	19.2	-	ns
Fall Time	t _f		-	8.2	-	ns
Gate Charge Characteristics ⁽⁷⁾						
Total Gate Charge (V _{GS} = 10V)	Q _g	V _{DS} = 50V, I _D = 20A V _{GS} = 10V	-	26	-	nC
Total Gate Charge (V _{GS} = 4.5V)	Q _g		-	13.3	-	nC
Gate-Source Charge	Q _{gs}		-	4.3	-	nC
Gate-Drain Charge	Q _{gd}		-	5.5	-	nC
Gate Plateau Voltage	V _{plateau}		-	3.0	-	V
Drain-Source Diode Characteristics ⁽⁷⁾						
Body Diode Reverse Recovery Time	t _{rr}	I _F = 20A, dI/dt = 100A/μs,	-	40	-	ns
Body Diode Reverse Recovery Charge	Q _{rr}	T _J = 25°C	-	50	-	nC
Diode Forward Current	I _S	T _C = 25°C	-	-	67	A

Notes:

1. This current is chip limited, which is calculated based on R_{thjc} .
2. This current is calculated on single pulse with 10us Single Pulse.
3. Defined by design, not subject to production test, E_{AS} condition: $T_J = 25^\circ\text{C}, V_{DD} = 50V, V_{GS} = 10V, L = 1.0\text{mH}$.
4. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
5. Thermal resistance from junction to the exposed pad.
6. Short duration pulse test used to minimize self-heating effect.
7. Defined by design, not subject to production.

Typical Electrical and Thermal Characteristics

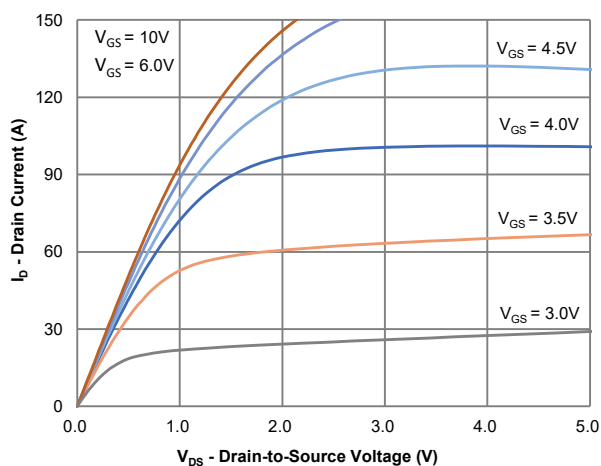


Figure 1: Output Characteristics

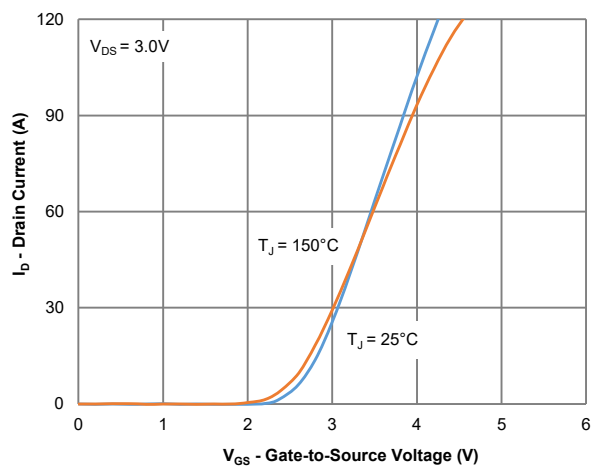


Figure 2: Transfer Characteristics

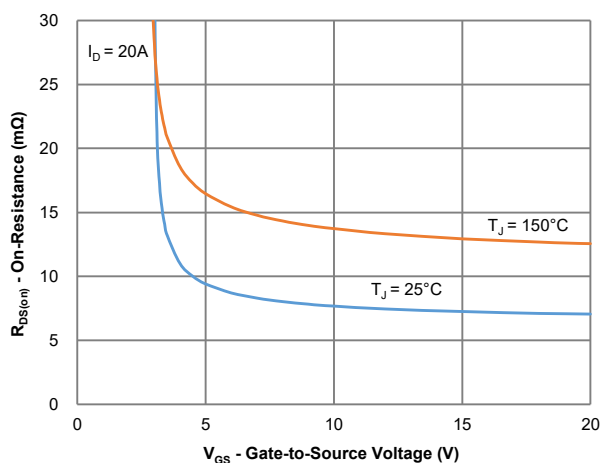


Figure 3: On-Resistance vs. Gate-Source Voltage

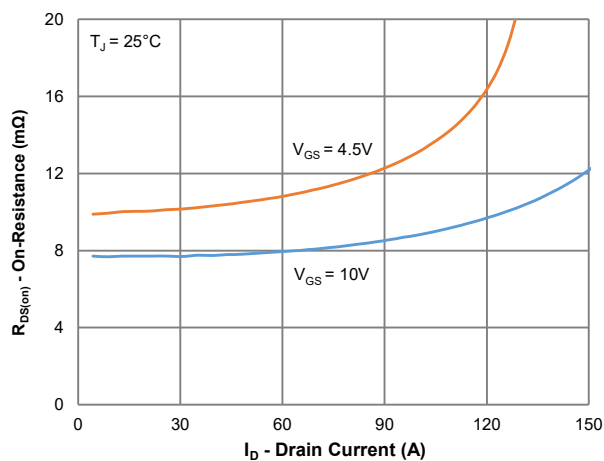


Figure 4: On-Resistance vs. Drain Current and Gate Voltage

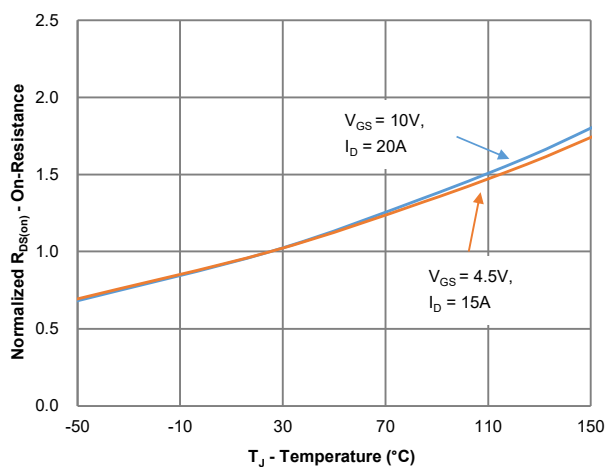


Figure 5: On-Resistance vs. Junction Temperature

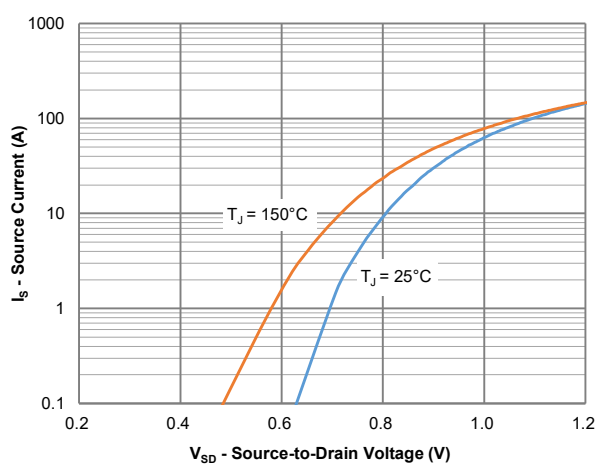
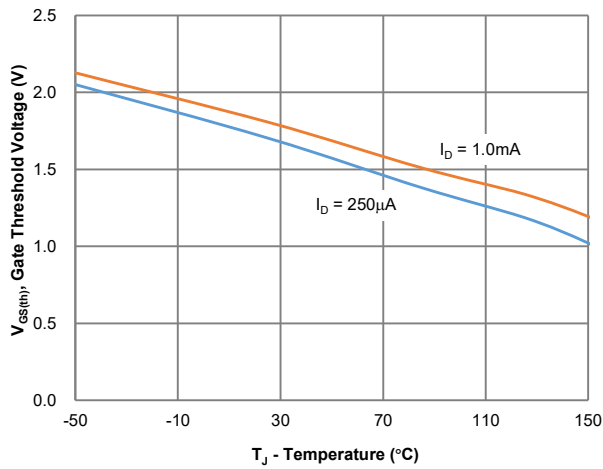
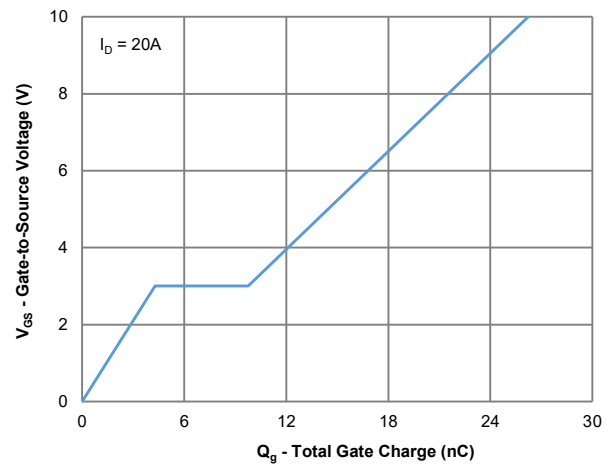
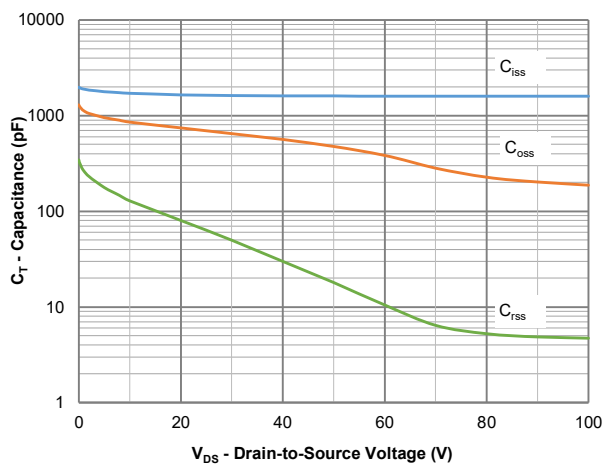
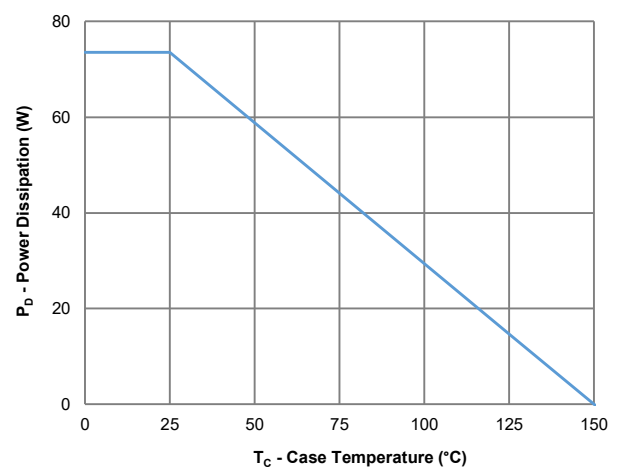
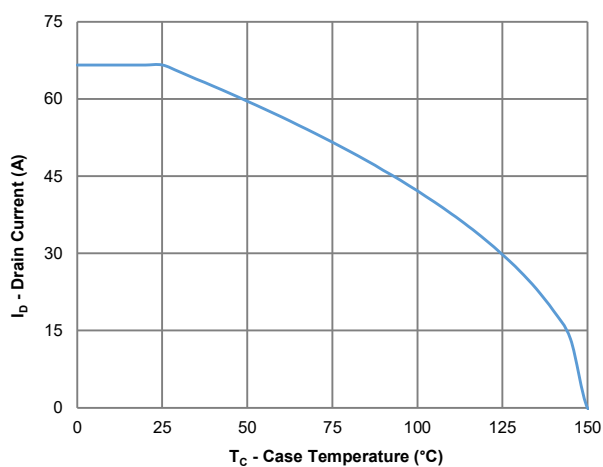
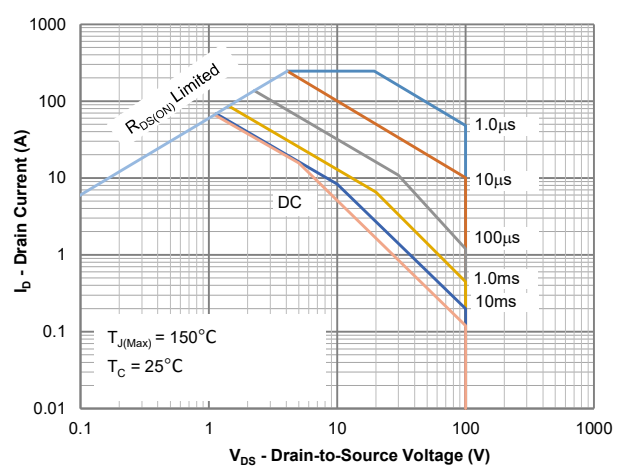


Figure 6: Source-Drain Diode Forward Voltage

Typical Electrical and Thermal Characteristics

Figure 7: Gate Threshold Variation vs. Junction Temperature

Figure 8: Gate Charge Characteristics

Figure 9: Capacitance Characteristics

Figure 10: Power Derating

Figure 11: Current Derating

Figure 12: Safe Operating Area

Typical Electrical and Thermal Characteristics

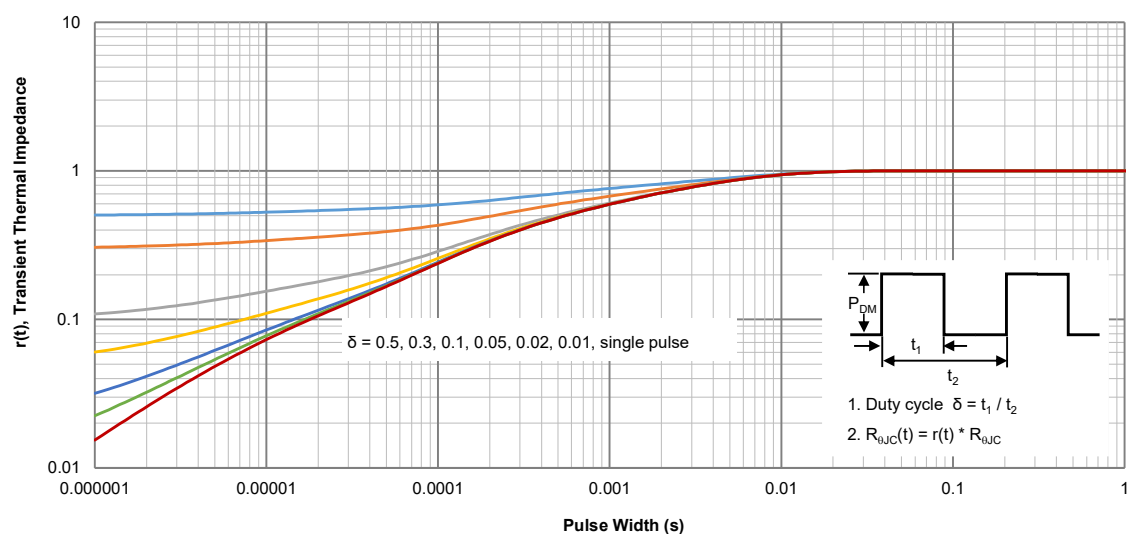
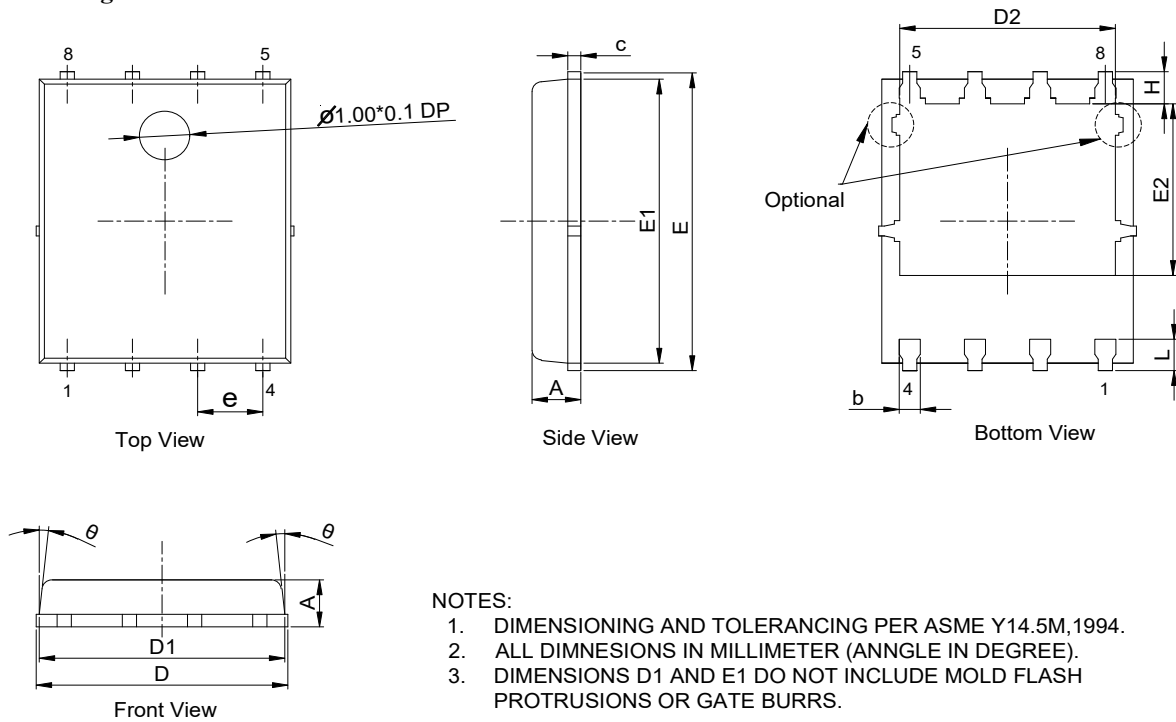


Figure 13: Normalized Maximum Transient Thermal Impedance

PDFN5060-8L Package Outline
Package Outline


DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.90	1.05	1.20
b	0.20	0.41	0.51
c	0.20	0.25	0.35
D	4.80	--	5.40
D1	4.65	--	5.30
D2	3.60	--	4.50
E	5.90	--	6.30
E1	5.60	--	6.00
E2	3.37	--	3.92
e	1.27BSC		
H	0.40	0.60	0.75
L	0.40	0.60	0.84
θ	0°	--	12°

Recommended Soldering Footprint
