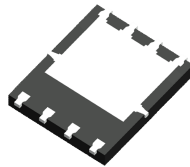


Product Summary

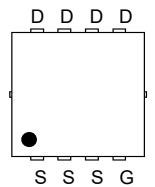
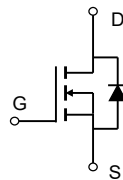
V_{DS}	$R_{DS(ON)_TYP}$	I_{D_MAX}
100 V	$3.6\text{ m}\Omega @ V_{GS} = 10V$	113 A

PDFN5060-8L


Top View



Bottom View


 PIN Configuration
(Top View)


Schematic Diagram

Features

- Low On-Resistance
- Excellent FoM (figure of merit)
- 100% ΔV_{DS} & UIS & Rg Tested


**HALOGEN
FREE**
Applications

- DC/DC in Telecoms and Industrial
- Synchronous Rectification in SMPS
- Hard Switching and High Speed Circuit

Mechanical Data

- Green Molding Compound
- Moisture Sensitivity: Level 1 per J-STD-020
- UL Flammability Classification Rating 94V-0

Ordering Information

Orderable Part Number	Package Type	Device Marking	Form	Quantity (pcs)
SMT10T03BHP	PDFN5060-8L	10T03BH	13" Tape&Reel	5,000

Maximum Ratings (@ $T_C = 25^\circ\text{C}$, unless otherwise specified.)

Parameter	Symbol	Value	Unit
Drain - Source Voltage	V_{DS}	100	V
Gate - Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($V_{GS} = 10V$) ⁽¹⁾	I_D	$T_C = 25^\circ\text{C}$ 113	A
		$T_C = 100^\circ\text{C}$ 71	A
Pulsed Drain Current ⁽²⁾	I_{DM}	450	A
Single Pulse Avalanche Energy ⁽³⁾	E_{AS}	578	mJ
Single Pulse Avalanche Current ($L = 0.1\text{mH}$)	I_{AS}	60	A
Power Dissipation	P_D	$T_C = 25^\circ\text{C}$ 104	W
		$T_C = 100^\circ\text{C}$ 42	W
Junction & Storage Temperature Range	T_J, T_{STG}	-55 ~ +150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance, Junction-to-Ambient ⁽⁴⁾	$R_{\theta JA}$	35	44	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Case ⁽⁵⁾	$R_{\theta JC}$	0.90	1.2	$^\circ\text{C/W}$

Electrical Characteristics (@ $T_J = 25^\circ\text{C}$, unless otherwise specified.)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Off Characteristics ⁽⁶⁾						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100V, V _{GS} = 0V	-	-	1.0	μA
		T _J = 125°C	-	-	100	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} = 0V	-	-	±100	nA
On Characteristics ⁽⁶⁾						
Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 250μA	2.0	3.0	4.0	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D = 20A	-	3.6	4.4	mΩ
Forward Transconductance	g _{fs}	V _{DS} = 5.0V, I _D = 20A	-	48	-	S
Diodes Forward Voltage	V _{SD}	I _S = 2.0A, V _{GS} = 0V	-	0.7	1.2	V
Dynamic Characteristics ⁽⁷⁾						
Input Capacitance	C _{iss}	V _{DS} = 50V, V _{GS} = 0V, f = 1MHz	-	3056	-	pF
Output Capacitance	C _{oss}		-	1379	-	pF
Reverse Transfer Capacitance	C _{rss}		-	19	-	pF
Gate Resistance	R _g	V _{GS} = 0V, V _{DS} = 0V, f = 1MHz	-	1.6	-	Ω
Switching Characteristics ⁽⁷⁾						
Turn-On DelayTime	t _{d(on)}	V _{GS} = 10V, V _{DS} = 50V I _D = 20A, R _{GEN} = 3.0Ω	-	9.2	-	ns
Rise Time	t _r		-	15	-	ns
Turn-Off DelayTime	t _{d(off)}		-	29	-	ns
Fall Time	t _f		-	19	-	ns
Gate Charge Characteristics ⁽⁷⁾						
Total Gate Charge (V _{GS} = 10V)	Q _g	V _{DS} = 50V, I _D = 20A V _{GS} = 10V	-	44	-	nC
Total Gate Charge (V _{GS} = 6.0V)	Q _g		-	28	-	nC
Gate-Source Charge	Q _{gs}		-	9.3	-	nC
Gate-Drain Charge	Q _{gd}		-	8.4	-	nC
Gate Plateau Voltage	V _{plateau}		-	3.4	-	V
Drain-Source Diode Characteristics ⁽⁷⁾						
Body Diode Reverse Recovery Time	t _{rr}	I _F = 20A, dI/dt = 100A/μs, T _J = 25°C	-	65	-	ns
Body Diode Reverse Recovery Charge	Q _{rr}		-	138	-	nC
Diode Forward Current	I _S	T _C = 25°C	-	-	113	A

Notes:

1. This current is chip limited, which is calculated based on R_{thjc} .
2. This current is calculated on single pulse with 10us Single Pulse.
3. Defined by design, not subject to production test, E_{AS} condition: $T_J = 25^\circ\text{C}, V_{DD} = 50V, V_{GS} = 10V, L = 1.0mH$.
4. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
5. Thermal resistance from junction to the exposed pad.
6. Short duration pulse test used to minimize self-heating effect.
7. Defined by design, not subject to production.

Typical Electrical and Thermal Characteristics

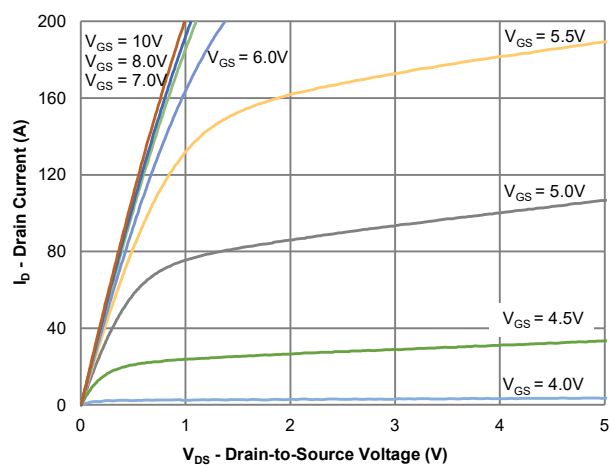


Figure 1: Output Characteristics

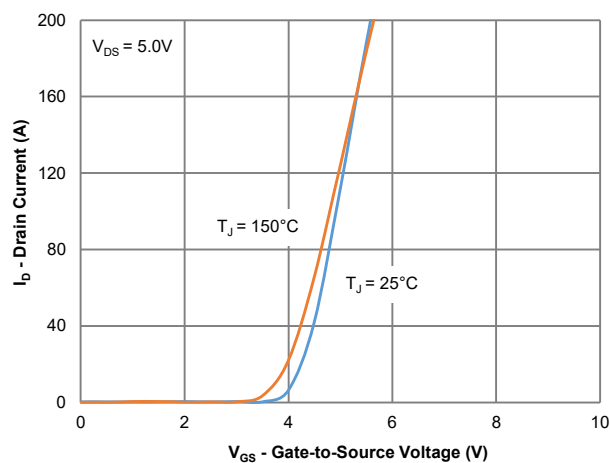


Figure 2: Transfer Characteristics

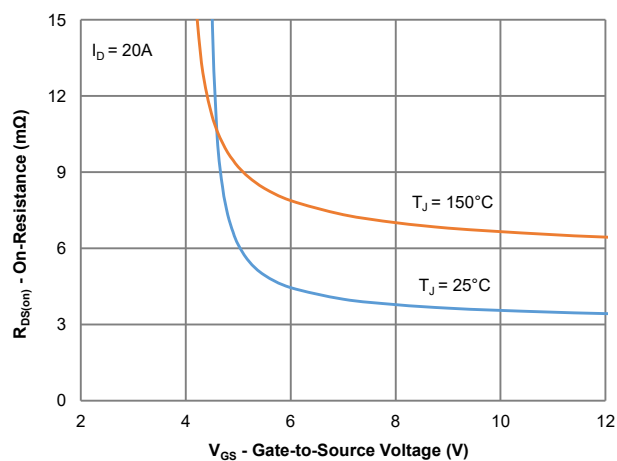


Figure 3: On-Resistance vs. Gate-Source Voltage

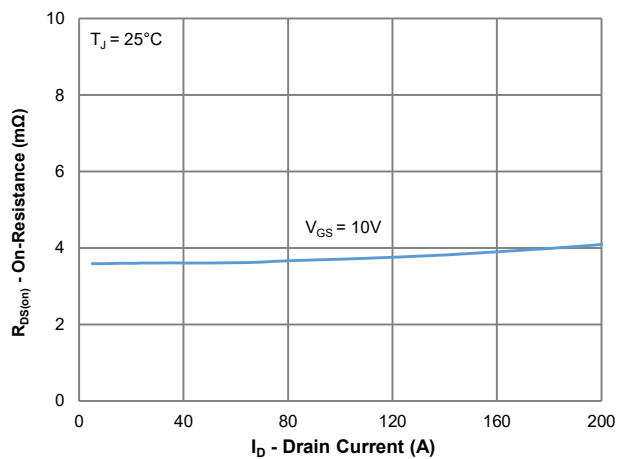


Figure 4: On-Resistance vs. Drain Current and Gate Voltage

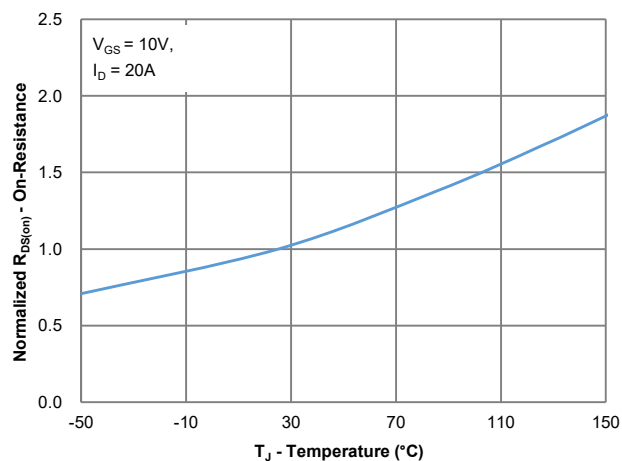


Figure 5: On-Resistance vs. Junction Temperature

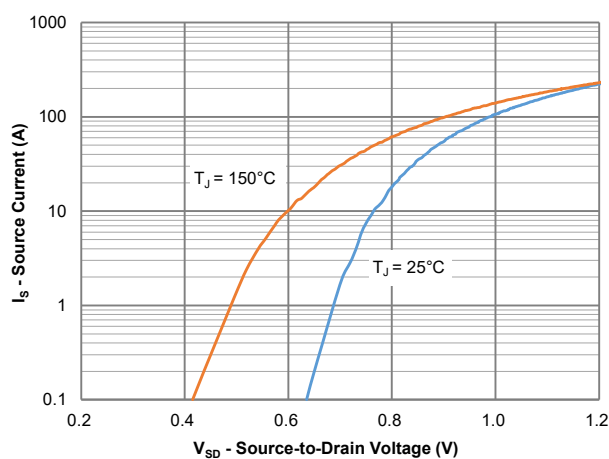


Figure 6: Source-Drain Diode Forward Voltage

Typical Electrical and Thermal Characteristics

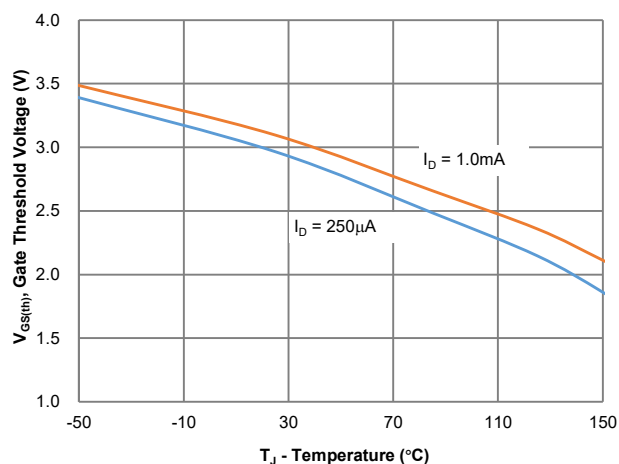


Figure 7: Gate Threshold Variation vs. Junction Temperature

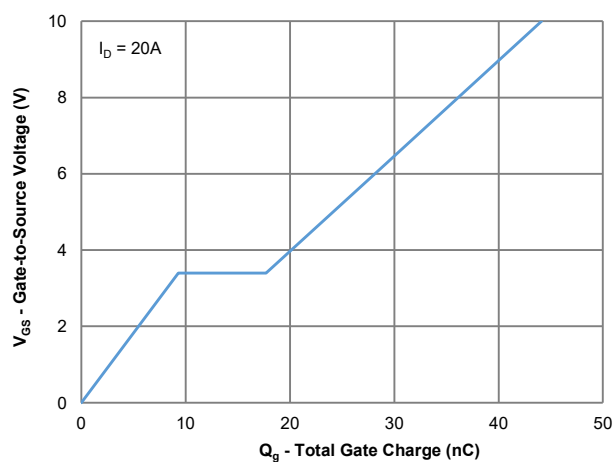


Figure 8: Gate Charge Characteristics

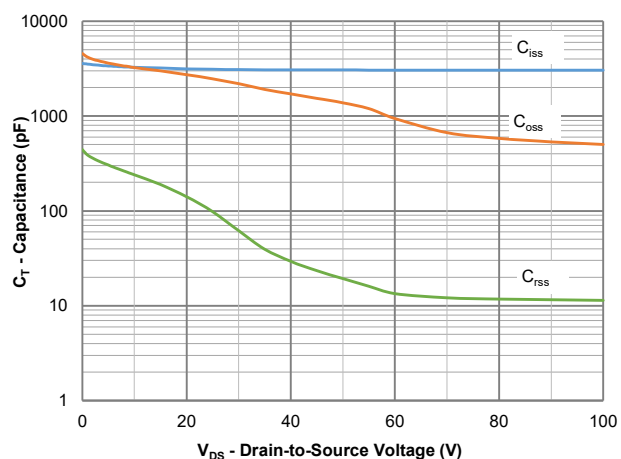


Figure 9: Capacitance Characteristics

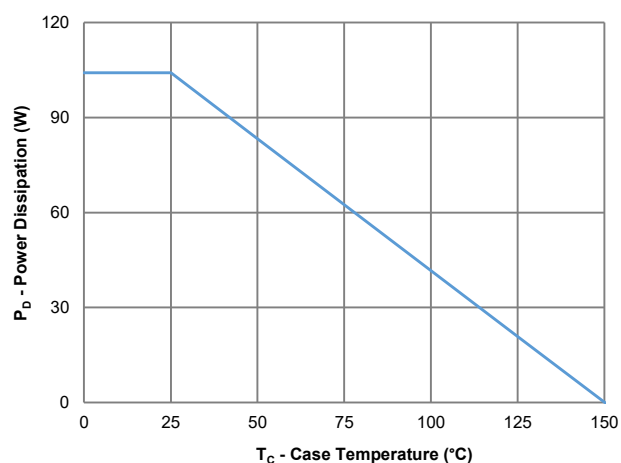


Figure 10: Power Derating

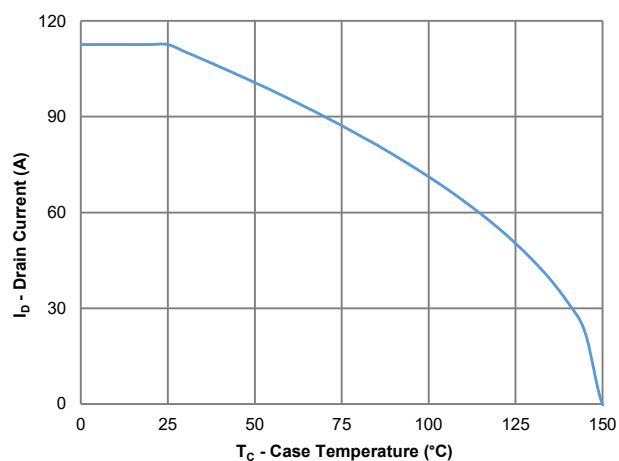


Figure 11: Current Derating

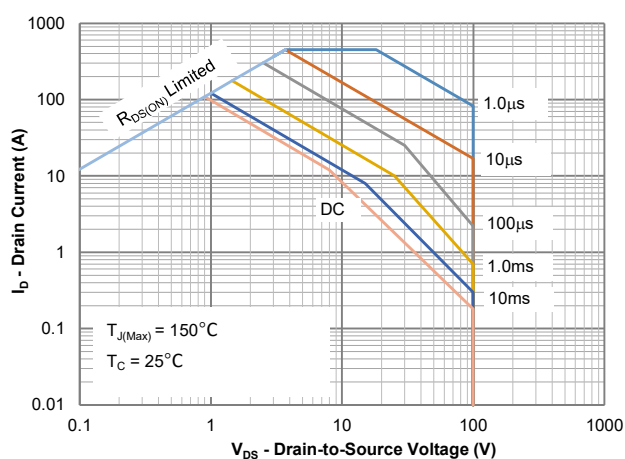
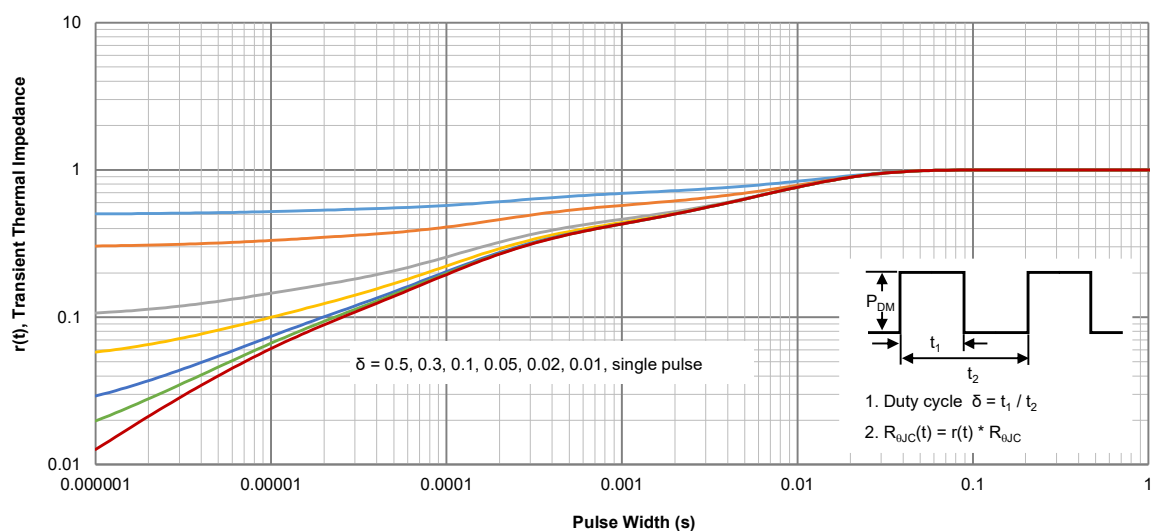
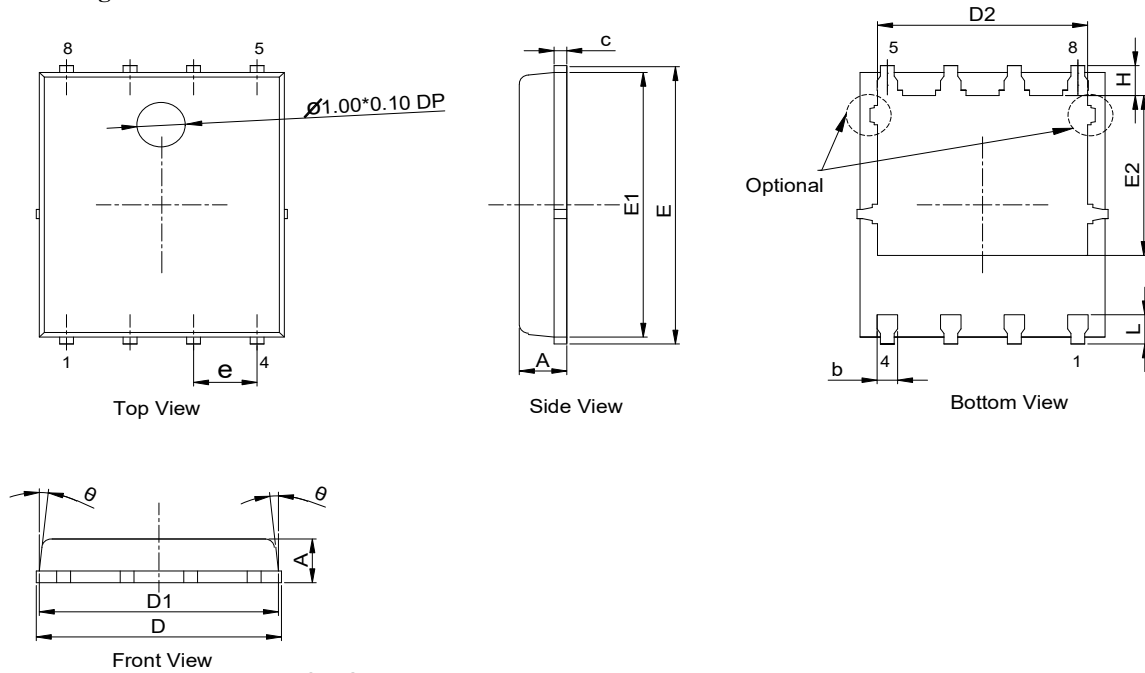


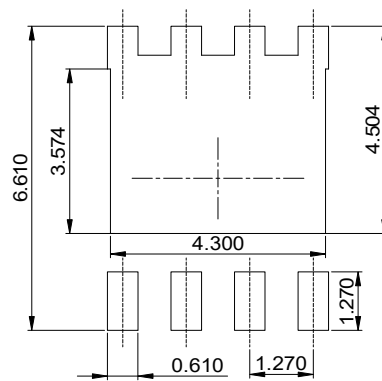
Figure 12: Safe Operating Area

Typical Electrical and Thermal Characteristics

Figure 13: Normalized Maximum Transient Thermal Impedance

PDFN5060-8L Package Outline
Package Outline

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. ALL DIMENSIONS IN MILLIMETER (ANGLE IN DEGREE).
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.90	1.05	1.20
b	0.20	0.41	0.51
c	0.20	0.25	0.35
D	4.80	--	5.40
D1	4.65	--	5.30
D2	3.60	--	4.30
E	5.90	--	6.30
E1	5.60	--	6.00
E2	3.37	--	3.92
e	1.27BSC		
H	0.40	0.60	0.75
L	0.40	0.60	0.84
theta	0°	--	12°

Recommended Soldering Footprint


DIMENSIONS: MILLIMETERS