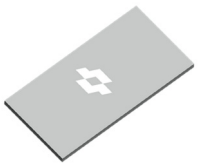
## Product Summary

| $V_{SS}$ | $R_{SS(ON)_TYP}$ | $I_{S_MAX}$ |
|---|---|---|
| 12 V | 2.1 mΩ @$V_{GS}$ = 4.5V | 29 A |
| | 2.2 mΩ @$V_{GS}$ = 3.8V | |
| | 2.6 mΩ @$V_{GS}$ = 3.1V | |
| | 3.2 mΩ @$V_{GS}$ = 2.5V | |

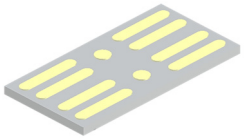
## Features

- Trench Technology
- ESD Protected Gate
- Common-Drain Type
- Supper High Density Cell Design
- Extremely Low Threshold Voltage
- Excellent Source to Source On-Resistance

**CSP3015-10**



Top View

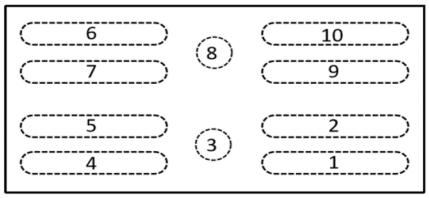


Bottom View

RoHS HALOGEN FREE Pb Pb-Free

## Applications

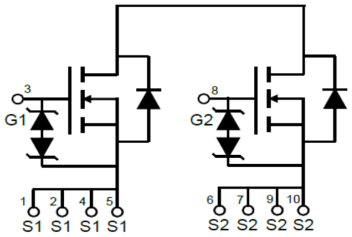
- Li-battery Protection Circuit




PIN Configuration
(Top View)

Source1:1,2,4,5 Gate1:3

Source2:6,7,9,10 Gate2:8




Schematic Diagram

## Ordering Information

| Orderable Part Number | Package Type | Device Marking | Form | Quantity (pcs) |
|---|---|---|---|---|
| SMN1202ACP10 | CSP3015-10 | 1202AP10 | 7" Tape&Reel | 3,000 |

## Maximum Ratings (@ $T_C$ = 25°C, unless otherwise specified.)

| Parameter | | Symbol | Value | Unit |
|---|---|---|---|---|
| Source - Source Voltage | | $V_{SS}$ | 12 | V |
| Gate - Source Voltage | | $V_{GS}$ | ±8 | V |
| Continuous Source Current ($V_{GS}$ = 4.5V) | $T_A$ = 25°C | $I_S$ (1) | 13.8 | A |
| | | $I_S$ (2) | 29 | A |
| Pulsed Source Current (3) | | $I_{SM}$ | 140 | A |
| Power Dissipation | $T_A$ = 25°C | $P_D$ (1) | 0.57 | W |
| | | $P_D$ (2) | 3.5 | W |
| Junction & Storage Temperature Range | | $T_J$, $T_{STG}$ | -55 ~ +150 | °C |

## Thermal Characteristics

| Parameter | Symbol | Typ. | Max. | Unit |
|---|---|---|---|---|
| Thermal Resistance, Junction-to-Ambient (1) | $R_{\theta JA}$ | 155 | 220 | °C/W |
| Thermal Resistance, Junction-to-Ambient (2) | $R_{\theta JA}$ | 30 | 36 | °C/W |

**Electrical Characteristics** (@ $T_J$ = 25°C, unless otherwise specified.)

| Parameter | Symbol | Test Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **Off Characteristics** (4) | | | | | | | |
| Source-Source Breakdown Voltage | $V_{SSS}$ | $V_{GS}$ = 0V, $I_D$ = 1.0mA | | 12 | - | - | V |
| Zero Gate Voltage Drain Current | $I_{SSS}$ | $V_{SS}$ = 12V, $V_{GS}$ = 0V | Test Circuit1 | - | - | 1.0 | μA |
| Gate-Source Leakage Current | $I_{GSS}$ | $V_{GS}$ = ±8.0V, $V_{SS}$ = 0V | Test Circuit2 | - | - | ±10 | μA |
| **On Characteristics** (4) | | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{SS}$ = 10V, $I_s$ = 1.1mA | Test Circuit3 | 0.5 | 0.9 | 1.4 | V |
| Static Source-Source On-Resistance | $R_{SS(ON)}$ | $V_{GS}$ = 4.5V, $I_S$ = 6.0A | Test Circuit4 | 1.5 | 2.1 | 2.7 | mΩ |
| | | $V_{GS}$ = 3.8V, $I_S$ = 6.0A | | 1.6 | 2.2 | 2.8 | mΩ |
| | | $V_{GS}$ = 3.1V, $I_S$ = 6.0A | | 1.7 | 2.6 | 3.9 | mΩ |
| | | $V_{GS}$ = 2.5V, $I_S$ = 6.0A | | 1.9 | 3.2 | 6.0 | mΩ |
| Diodes Forward Voltage | $V_{F(S-S)}$ | $I_S$ = 2.0A, $V_{GS}$ = 0V | Test Circuit7 | - | 0.7 | 1.0 | V |
| **Switching Characteristics** (5) | | | | | | | |
| Turn-On DelayTime | $t_{d(on)}$ | $V_{GS}$ = 4.5V, $V_{SS}$ = 6.0V<br>$I_S$ = 6.0A, $R_{GEN}$ = 3.0Ω | Test Circuit5 | - | 0.5 | - | μs |
| Rise Time | $t_r$ | | | - | 1.8 | - | μs |
| Turn-Off DelayTime | $t_{d(off)}$ | | | - | 3.0 | - | μs |
| Fall Time | $t_f$ | | | - | 6.3 | - | μs |
| **Gate Charge Characteristics** (5) | | | | | | | |
| Total Gate Charge ($V_{GS}$ = 4.5V) | $Q_g$ | $V_{GS}$ = 4.5V, $V_{SS}$ = 6.0V<br>$I_S$ = 6.0A | Test Circuit6 | - | 31 | - | nC |
| Gate-Source Charge | $Q_{gs}$ | | | - | 7.4 | - | nC |
| Gate-Drain Charge | $Q_{gd}$ | | | - | 8.7 | - | nC |

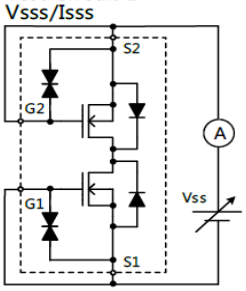
**Notes:**

1. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
2. Device mounted on Ceramic substrate (70mm X 70mm X t1.0mm, 2oz Copper) fully covered with copper.
3. This current is calculated on single pulse with 10μs Pulse & Duty Cycle = 1%.
4. Short duration pulse test used to minimize self-heating effect.
5. Defined by design, not subject to production.

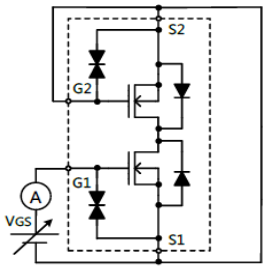
**Test Circuit**

**FET1 and the FET2 are both measured. Test circuits are example of measuring the FET1 side**

Test Circuit 1
Vsss/Isss

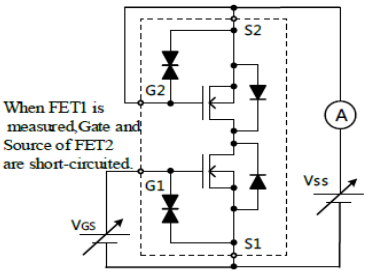



Test Circuit 2
IGSS

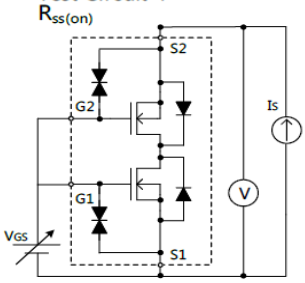



When FET1 is measured, Gate and Source of FET2 are short-circuited.

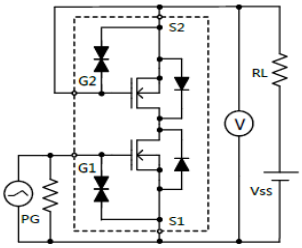
Test Circuit 3
VGS(th)



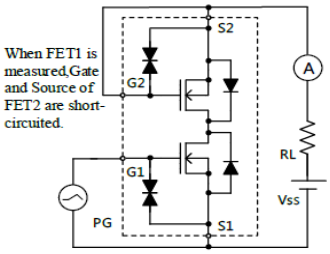

Test Circuit 4
Rss(on)



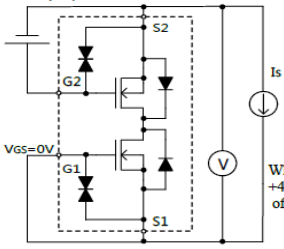

Test Circuit 5
td(on), tr, td(off), tf




Test Circuit 6
Qg




Test Circuit 7
VF(S-S)




When FET1 is measured, +4.5V is added to VGS of FET2.

## Typical Electrical and Thermal Characteristics

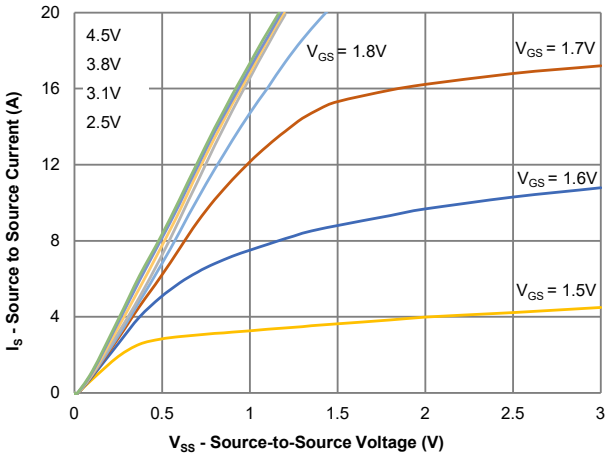



Figure 1: Output Characteristics

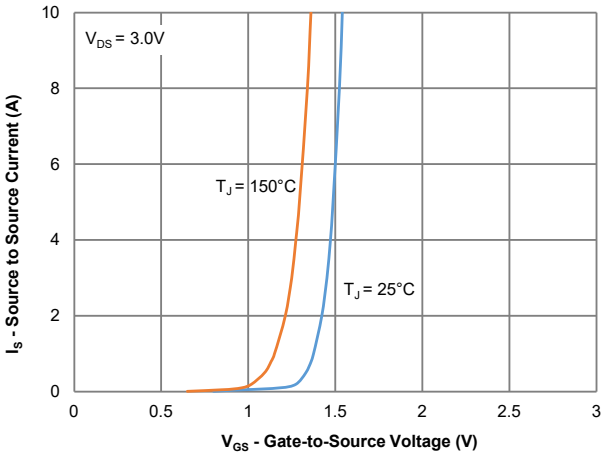



Figure 2: Transfer Characteristics

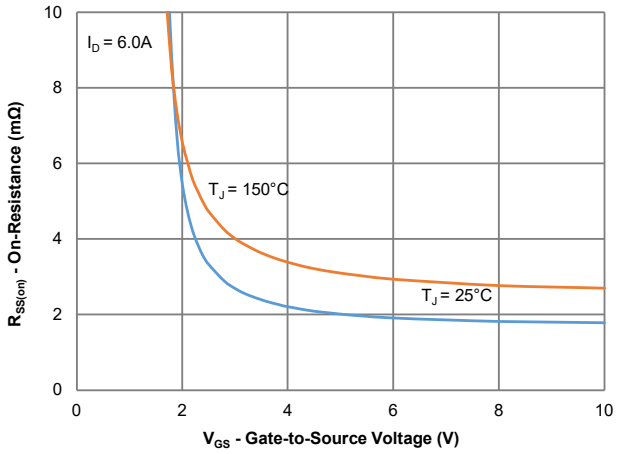



Figure 3: On-Resistance vs. Gate-Source Voltage

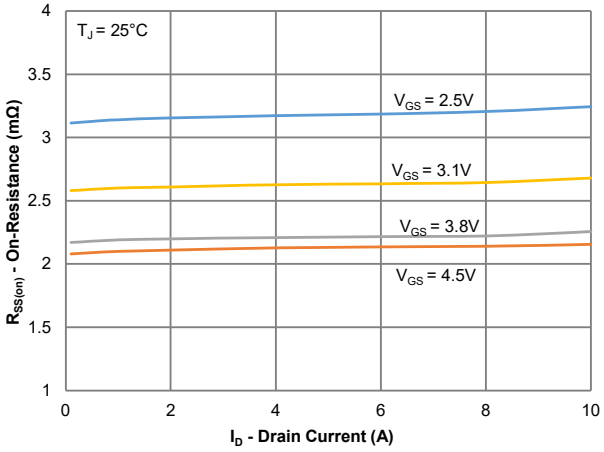



Figure 4: On-Resistance vs. Drain Current and Gate Voltage

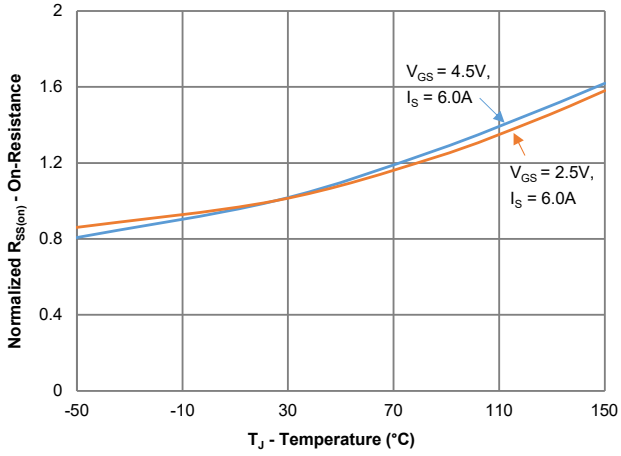



Figure 5: On-Resistance vs. Junction Temperature

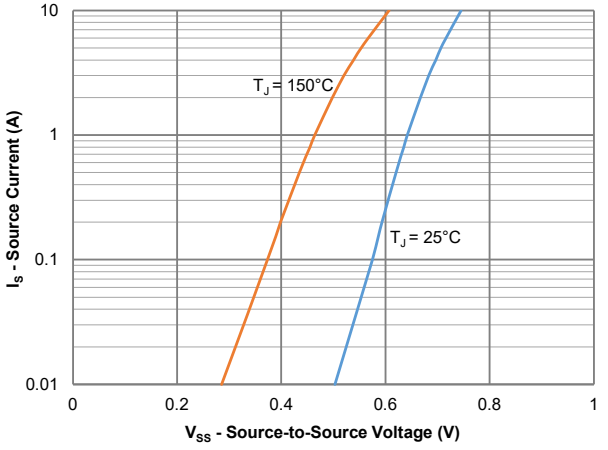



Figure 6: Source-Source Diode Forward Voltage

## Typical Electrical and Thermal Characteristics

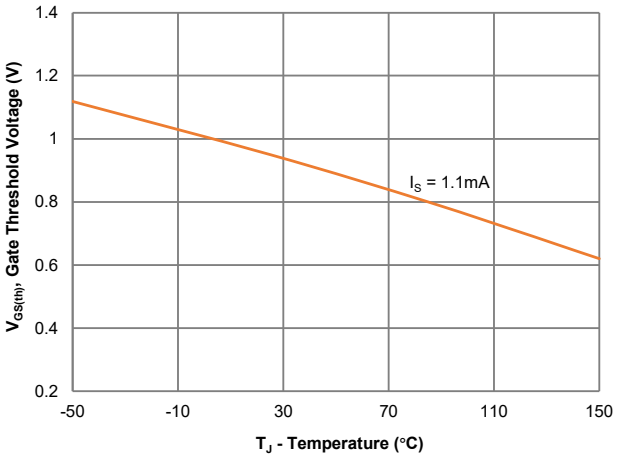



Figure 7: Gate Threshold Variation vs. Junction Temperature

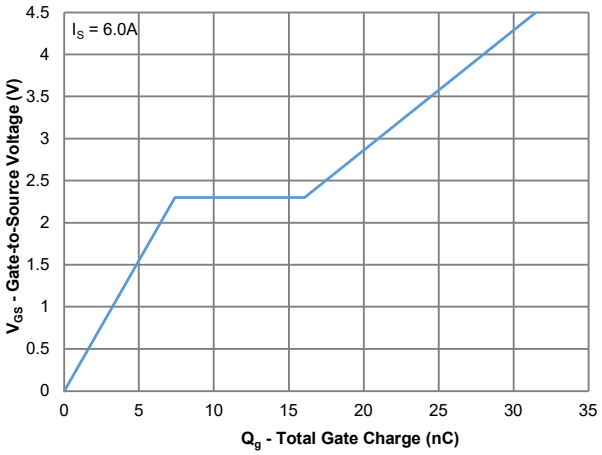



Figure 8: Gate Charge Characteristics

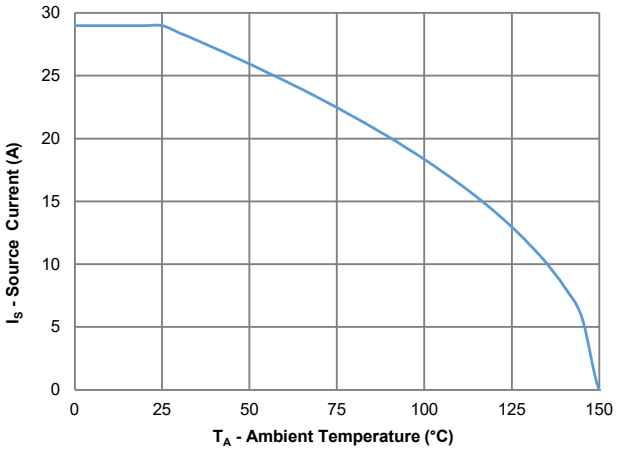



Figure 9: Current Derating

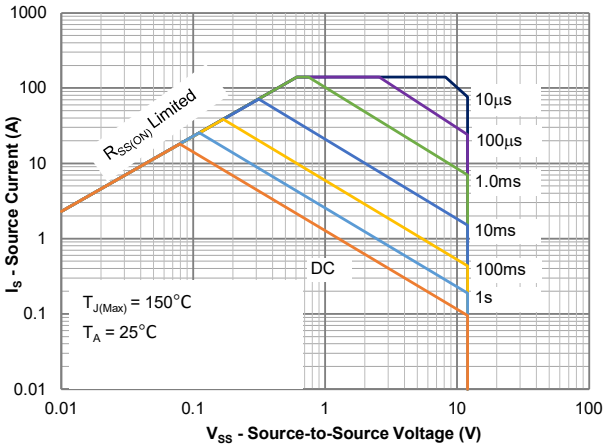



Figure 10: Safe Operating Area

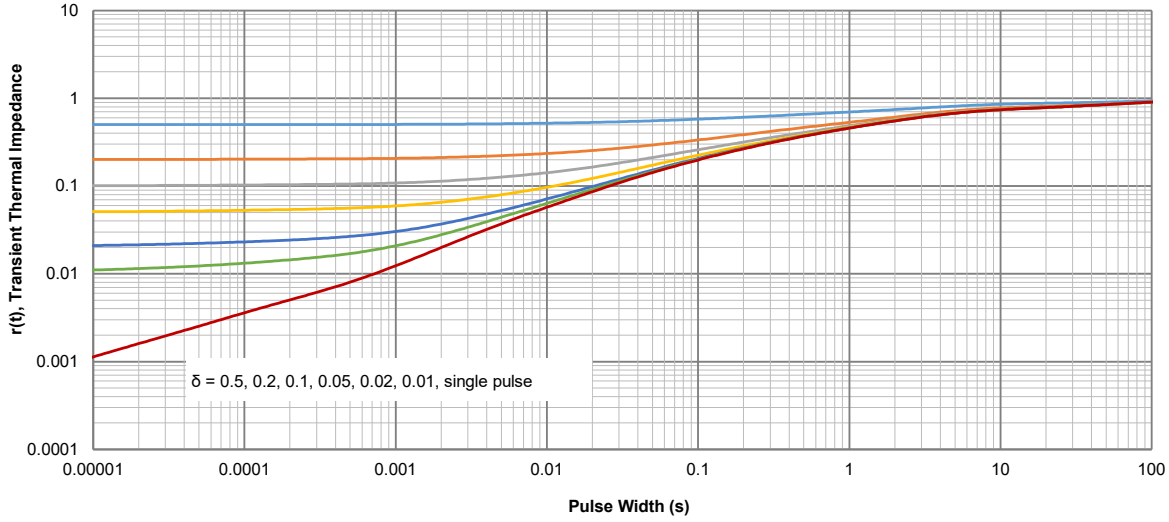
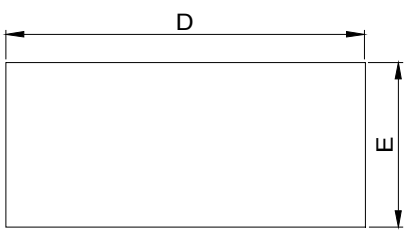


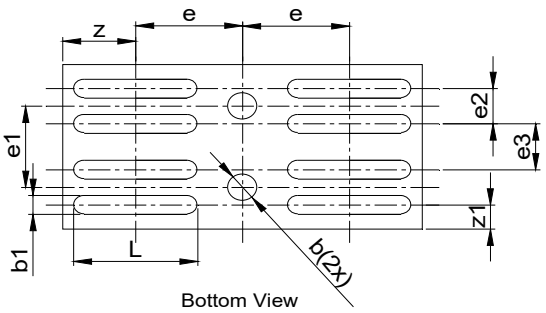

Figure 11: Normalized Maximum Transient Thermal Impedance

**CSP-10 Package Outline**

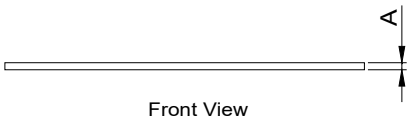
## Package Outline




Top View



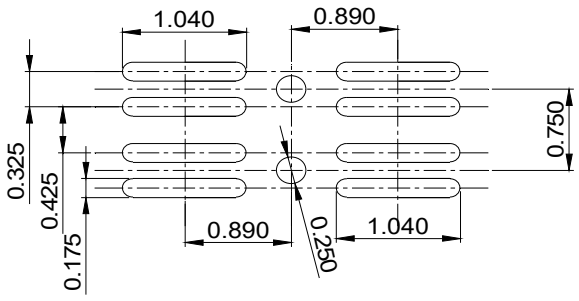

Bottom View




Front View

| DIM. | MILLIMETER | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.083 | 0.110 | 0.153 |
| b | 0.220 | 0.250 | 0.280 |
| b1 | 0.145 | 0.175 | 0.205 |
| D | 2.970 | 3.010 | 3.050 |
| E | 1.480 | 1.520 | 1.560 |
| e | 0.895BSC | | |
| e1 | 0.750BSC | | |
| e2 | 0.325BSC | | |
| e3 | 0.425BSC | | |
| Z | 0.610 | | |
| Z1 | 0.223 | | |
| L | 1.010 | 1.040 | 1.070 |

## Recommended Soldering Footprint




DIMENSIONS:MILLIMETERS