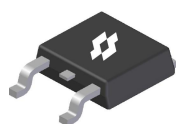
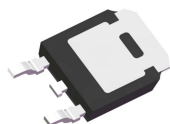


Product Summary

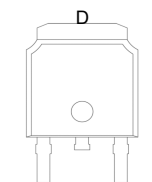
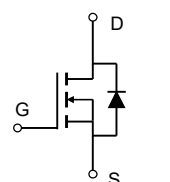
V_{DS}	$R_{DS(ON)_MAX}$	I_{D_MAX}
650 V	1.25 Ω @ $V_{GS} = 10V$	3.5 A

TO252-3L


Top View



Bottom View


 PIN Configuration
(Top View)


Schematic Diagram

Features

- Low On-Resistance
- Fast Switching Capability
- 100% UIS and R_g tested


Applications

- LED Lighting
- Charger and Adapter
- PC and Telecom Power

Mechanical Data

- Green Molding Compound
- Moisture Sensitivity: Level 3 per J-STD-020
- UL Flammability Classification Rating 94V-0

Ordering Information

Orderable Part Number	Package Type	Device Marking	Form	Quantity (pcs)
SMJ65R1K3ANU	TO252-3L	65R1K3AN	13" Tape&Reel	2,500

Maximum Ratings (@ $T_C = 25^\circ\text{C}$, unless otherwise specified.)

Parameter	Symbol	Value	Unit
Drain - Source Voltage	V_{DS}	650	V
Gate - Source Voltage	V_{GS}	± 30	V
Continuous Drain Current ($V_{GS} = 10V$) ⁽¹⁾	I_D	$T_C = 25^\circ\text{C}$ 3.5	A
		$T_C = 100^\circ\text{C}$ 2.2	A
Pulsed Drain Current ⁽²⁾	I_{DM}	11.8	A
Single Pulse Avalanche Energy ⁽³⁾	E_{AS}	62	mJ
Single Pulse Avalanche Current ($L = 10.0\text{mH}$)	I_{AS}	2.8	A
Power Dissipation	P_D	$T_C = 25^\circ\text{C}$ 42	W
		$T_C = 100^\circ\text{C}$ 16.7	W
MOSFET dv/dt Ruggedness, $V_{DS}=0\dots 480V$	dv/dt	50	V/ns
Reverse Diodes dv/dt, $V_{DS}=0\dots 480V$, $I_{SD} \leq I_D$	dv/dt	15	V/ns
Junction & Storage Temperature Range	T_J, T_{STG}	-55 ~ +150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance, Junction-to-Ambient ⁽⁴⁾	$R_{\theta JA}$	50	62	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Case ⁽⁵⁾	$R_{\theta JC}$	2.3	3.0	$^\circ\text{C/W}$

Electrical Characteristics (@ $T_J = 25^\circ\text{C}$, unless otherwise specified.)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Off Characteristics ⁽⁶⁾						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	650	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 650V, V _{GS} = 0V	-	-	1.0	μA
		T _J = 125°C	-	-	100	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} = ±30V, V _{DS} = 0V	-	-	±100	nA
On Characteristics ⁽⁶⁾						
Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 250μA	2.5	3.5	4.5	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D = 2.0A	-	1.05	1.25	Ω
Forward Transconductance	g _{fs}	V _{DS} = 5.0V, I _D = 2.0A	-	2.9	-	S
Diodes Forward Voltage	V _{SD}	I _S = 2.0A, V _{GS} = 0V	-	0.85	1.2	V
Dynamic Characteristics ⁽⁷⁾						
Input Capacitance	C _{iss}	V _{DS} = 50V, V _{GS} = 0V, f = 1.0MHz	-	235	-	pF
Output Capacitance	C _{oss}		-	25	-	pF
Reverse Transfer Capacitance	C _{rss}		-	6.1	-	pF
Effective Output Capacitance, Energy Related ⁽⁸⁾	C _{O(er)}	V _{GS} =0V,	-	15.3	-	pF
Effective Output Capacitance, Time Related ⁽⁹⁾	C _{O(tr)}	V _{DS} =0...480V, f = 1.0MHz	-	55	-	pF
Gate Resistance	R _g	V _{GS} = 0V, V _{DS} = 0V, f = 1.0MHz	-	10.0	-	Ω
Switching Characteristics ⁽⁷⁾						
Turn-On DelayTime	t _{d(on)}	V _{GS} = 10V, V _{DS} = 400V I _D = 2.0A, R _{GEN} = 3.0Ω	-	8.2	-	ns
Rise Time	t _r		-	7.7	-	ns
Turn-Off DelayTime	t _{d(off)}		-	19.3	-	ns
Fall Time	t _f		-	22	-	ns
Gate Charge Characteristics ⁽⁷⁾						
Total Gate Charge (V _{GS} = 10V)	Q _g	V _{DS} = 400V, I _D = 2.0A V _{GS} = 10V	-	6.1	-	nC
Total Gate Charge (V _{GS} = 6.0V)	Q _g		-	4.1	-	nC
Gate-Source Charge	Q _{gs}		-	1.3	-	nC
Gate-Drain Charge	Q _{gd}		-	2.6	-	nC
Gate Plateau Voltage	V _{plateau}		-	5.3	-	V
Drain-Source Diode Characteristics ⁽⁷⁾						
Body Diode Reverse Recovery Time	t _{rr}	I _F = 2.0A, dI/dt = 100A/μs, T _J = 25°C	-	137	-	ns
Body Diode Reverse Recovery Charge	Q _{rr}		-	0.75	-	μC
Body Diode Reverse Recovery Current	I _{rrm}		-	10.4	-	A
Diode Forward Current	I _S	T _C = 25°C	-	-	3.5	A

Notes:

1. This current is chip limited, which is calculated based on R_{thjc} .
2. This current is calculated on single pulse with 10 μs Pulse & Duty Cycle = 1%.
3. Defined by design, not subject to production test, E_{AS} condition: $T_J=25^\circ\text{C}, V_{DS}=400V, V_{GS}=10V, L=30mH$.
4. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
5. Thermal resistance from junction to soldering point (on the exposed drain pad).
6. Short duration pulse test used to minimize self-heating effect.
7. Defined by design, not subject to production.
8. $C_{O(er)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 480V.
9. $C_{O(tr)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 480V.

Typical Electrical and Thermal Characteristics

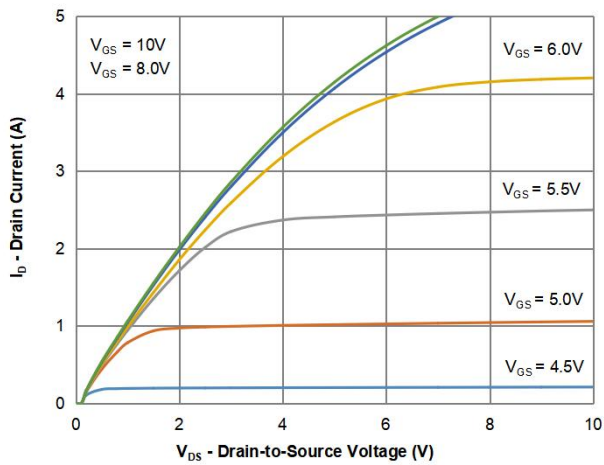


Figure 1: Output Characteristics

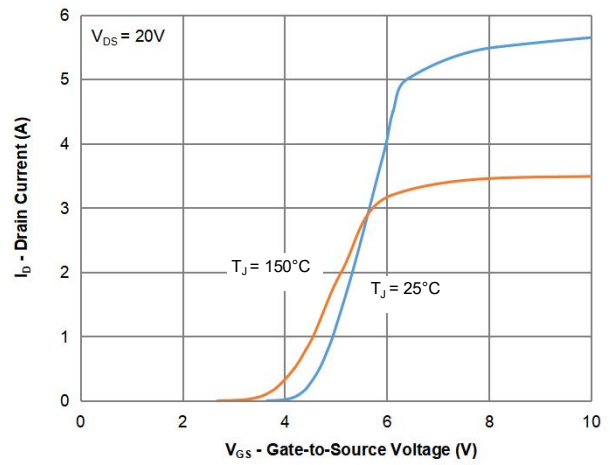


Figure 2: Transfer Characteristics

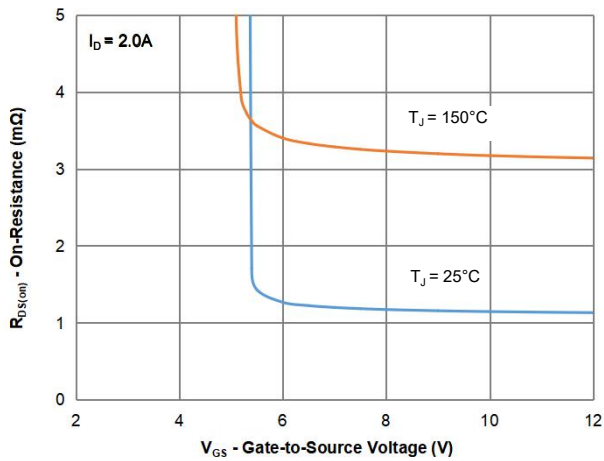


Figure 3: On-Resistance vs. Gate-Source Voltage

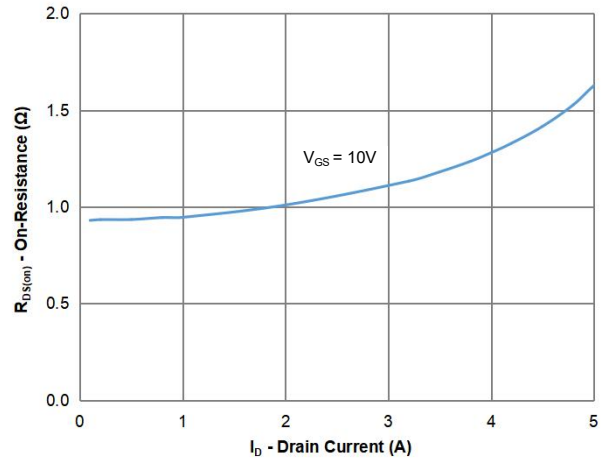


Figure 4: On-Resistance vs. Drain Current

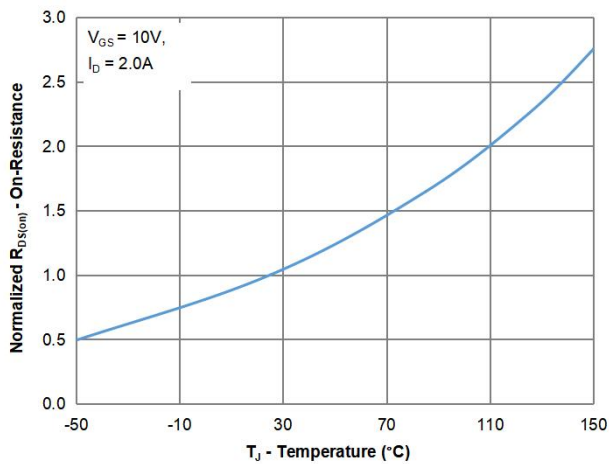


Figure 5: On-Resistance vs. Junction Temperature

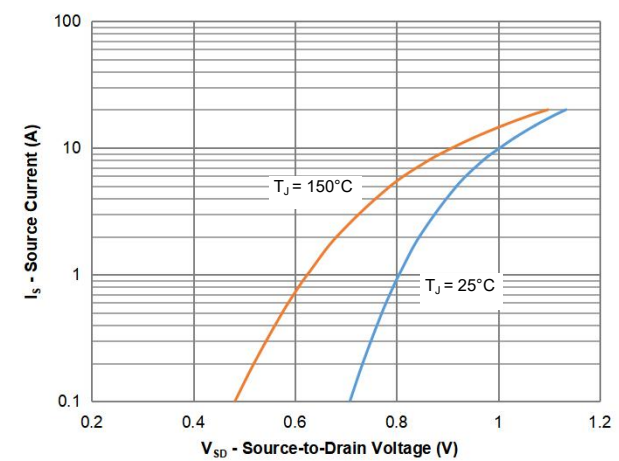


Figure 6: Source-Drain Diode Forward Voltage

Typical Electrical and Thermal Characteristics

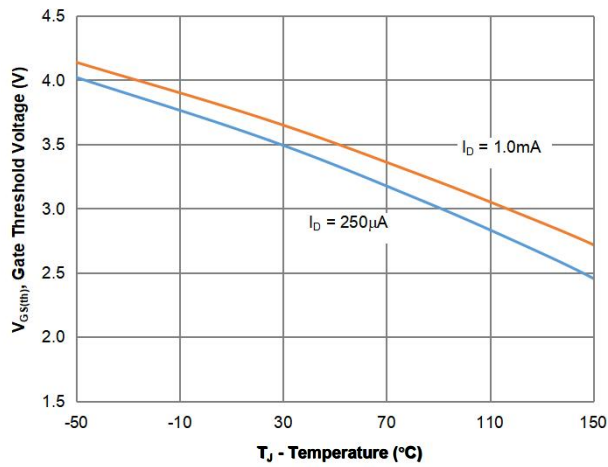


Figure 7: Gate Threshold Variation vs. Junction Temperature

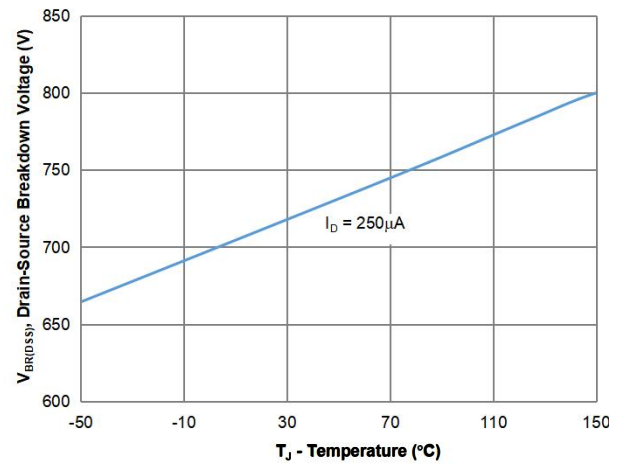


Figure 8: $V_{BR(DSS)}$ vs. Junction Temperature

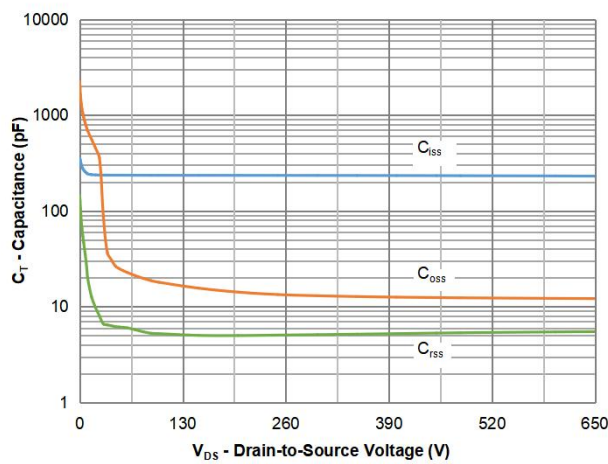


Figure 9: Capacitance Characteristics

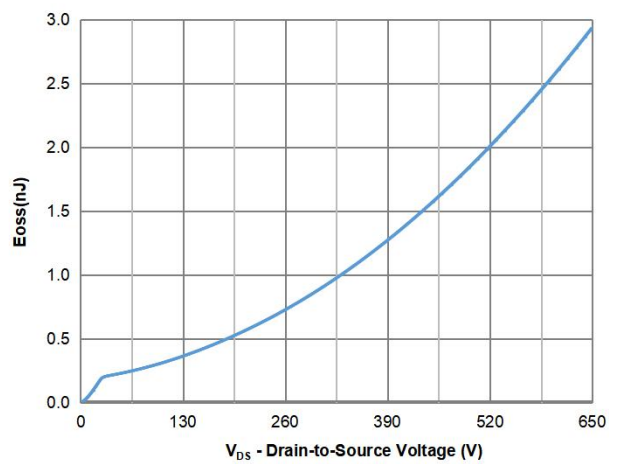


Figure 10: C_{oss} Stored Energy

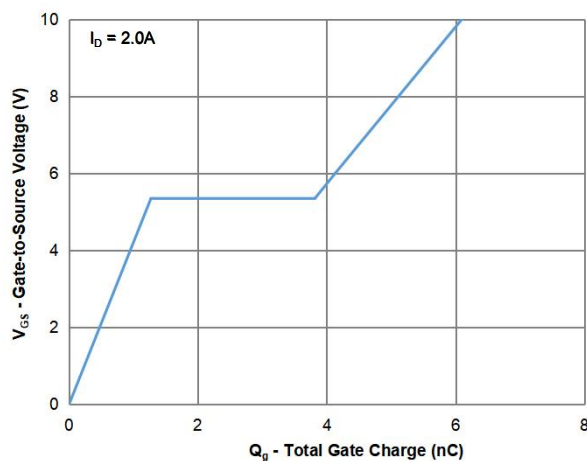


Figure 11: Gate Charge Characteristics

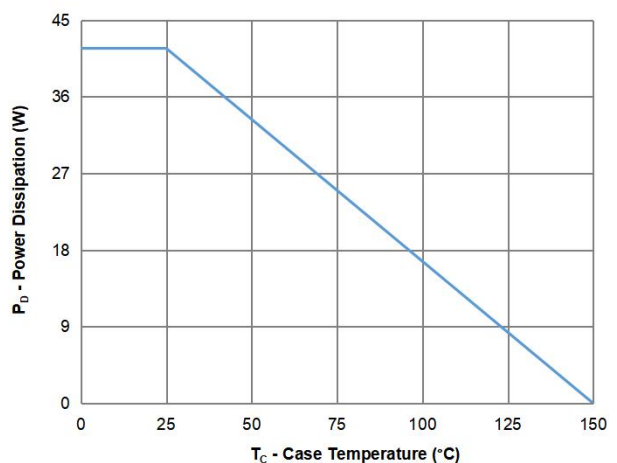


Figure 12: Power Derating

Typical Electrical and Thermal Characteristics

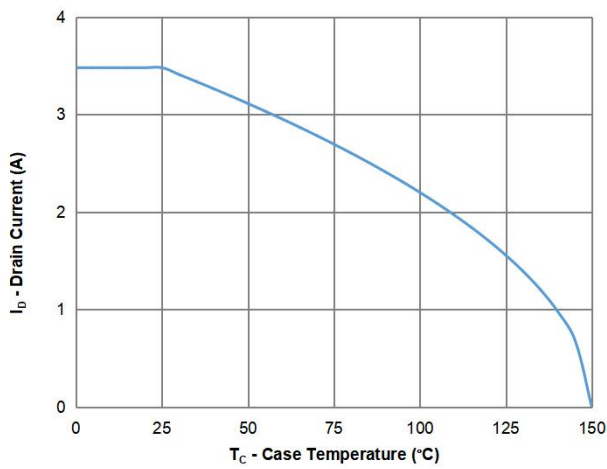


Figure 13: Current Derating

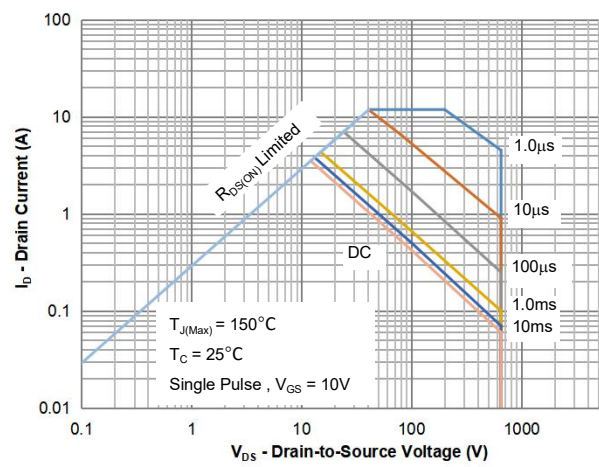


Figure 14: Safe Operating Area

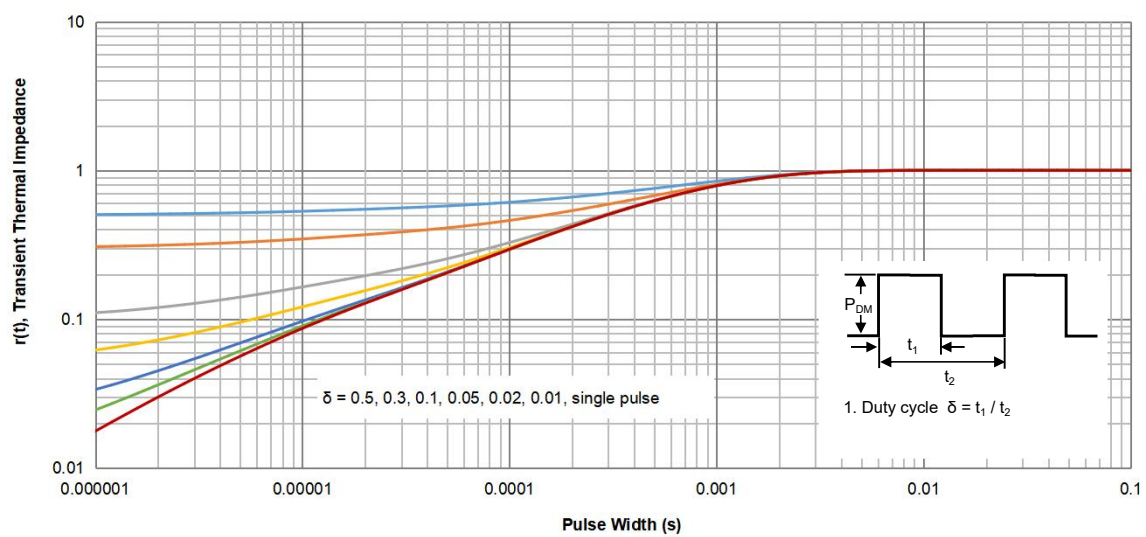
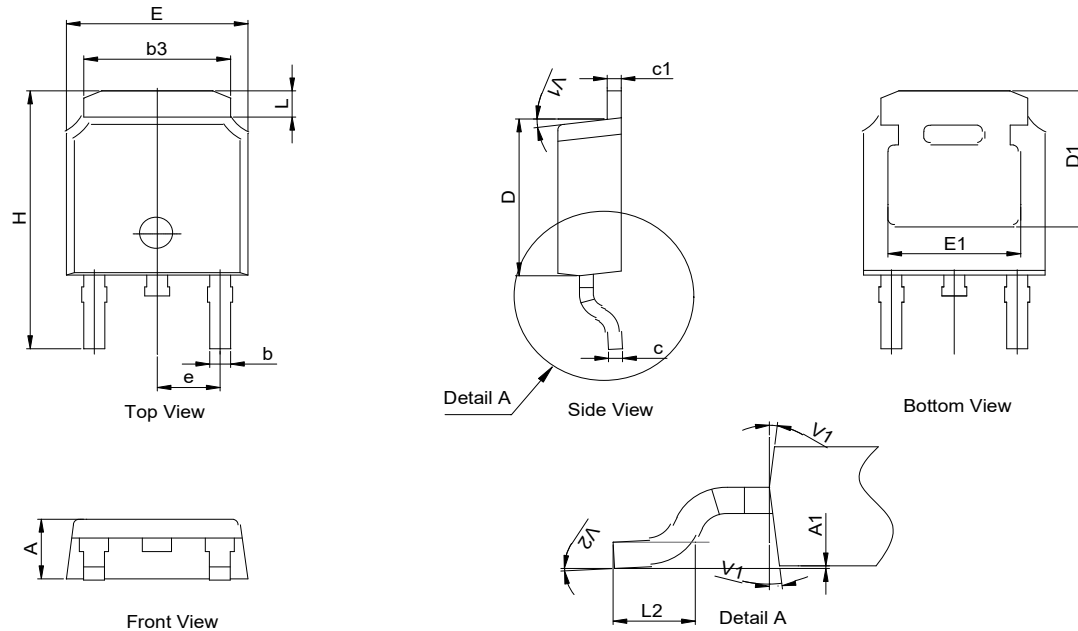
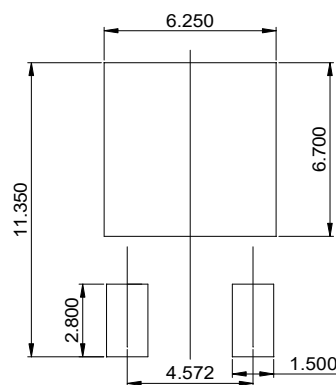


Figure 15: Normalized Maximum Transient Thermal Impedance

TO252-3L Package Outline
Package Outline


DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	0	-	0.13
b	0.62	0.76	0.90
c	0.40	0.50	0.61
c1	0.46	0.50	0.58
D	5.97	6.10	6.23
D1	5.05	--	--
E	6.35	6.60	6.73
E1	4.32	--	--
b3	5.21	5.38	5.55
e	2.29 BSC		
H	9.40	10.00	10.40
L	0.89	--	1.27
L2	1.40		1.78
V1	7° REF		
V2	0°	-	6°

Recommend Soldering Footprint


DIMENSIONS:MILLIMETERS