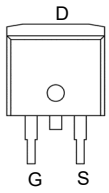
Product Summary

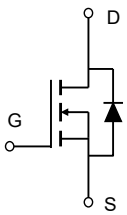
V_{DS}	$R_{DS(ON)_MAX}$	I_{D_MAX}
650 V	190 mΩ @V_{GS} = 10V	20.0 A

TO263-3L

Top View



PIN Configuration
(Top View)



Schematic Diagram

Features

- Low On-Resistance
- Fast Switching Capability
- 100% ΔVDS & UIS & Rg Tested

RoHS HALOGEN FREE

Applications

- LED Lighting
- Charger and Adapter
- PC and Telecom Power

Mechanical Data

- Green Molding Compound
- Moisture Sensitivity: Level 3 per J-STD-020
- UL Flammability Classification Rating 94V-0

Ordering Information

Orderable Part Number	Package Type	Device Marking	Form	Quantity (pcs)
SMJ65R190BNT	TO263-3L	65R190B	13" Tape&Reel	1,000

Maximum Ratings (@ T_C = 25°C, unless otherwise specified.)

Parameter		Symbol	Value	Unit
Drain - Source Voltage		V_{DS}	650	V
Gate - Source Voltage		V_{GS}	±30	V
Continuous Drain Current (V_{GS} = 10V) (1)	T_C = 25°C	I_D	20	A
	T_C = 100°C		10.5	A
Pulsed Drain Current (2)		I_{DM}	60	A
Single Pulse Avalanche Energy (3)		E_{AS}	794	mJ
Single Pulse Avalanche Current (L= 10.0mH)		I_{AS}	9.1	A
Power Dissipation	T_C = 25°C	P_D	144	W
	T_C = 100°C		57.5	W
MOSFET dv/dt Ruggedness, V_{DS}=0…400V		dv/dt	50	V/ns
Reverse Diodes dv/dt, V_{DS}=0…400V, I_{SD}≤I_D		dv/dt	50	V/ns
Junction & Storage Temperature Range		T_J, T_{STG}	-55 ~ +150	°C

Thermal Characteristics

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance, Junction-to-Ambient (4)	$R_{\theta JA}$	50	65	°C/W
Thermal Resistance, Junction-to-Case (5)	$R_{\theta JC}$	0.67	0.87	°C/W

Electrical Characteristics (@ T_J = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Off Characteristics [6]						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	650	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 600V, V_{GS} = 0V	-	-	1.0	μA
		T_J = 125°C	-	-	100	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±30V, V_{DS} = 0V	-	-	±100	nA
On Characteristics [6]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250μA	3.0	4.0	5.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 10A	-	169	190	mΩ
Diodes Forward Voltage	V_{SD}	I_S = 10A, V_{GS} = 0V	-	0.83	1.2	V
Dynamic Characteristics [7]						
Input Capacitance	C_{iss}	V_{DS} = 100V, V_{GS} = 0V, f = 1MHz	-	1658	-	pF
Output Capacitance	C_{oss}		-	60	-	pF
Reverse Transfer Capacitance	C_{rss}		-	5.0	-	pF
Effective Output Capacitance, Energy Related [8]	$C_{O(er)}$	V_{GS}=0V, V_{DS}=0...480V, f = 1MHz	-	58	-	pF
Effective Output Capacitance, Time Related [9]	$C_{O(tr)}$		-	239	-	pF
Gate Resistance	R_g	V_{GS} = 0V, V_{DS} = 0V, f = 1MHz	-	17	-	Ω
Switching Characteristics [7]						
Turn-On DelayTime	$t_{d(on)}$	V_{GS} = 10V, V_{DS} = 400V I_D = 10A, R_{GEN} = 3.0Ω	-	57	-	ns
Rise Time	t_r		-	53	-	ns
Turn-Off DelayTime	$t_{d(off)}$		-	152	-	ns
Fall Time	t_f		-	30	-	ns
Gate Charge Characteristics [7]						
Total Gate Charge (V_{GS} = 10V)	Q_g	V_{DS} = 400V, I_D = 10A V_{GS} = 10V	-	39	-	nC
Total Gate Charge (V_{GS} = 8.0V)	Q_g		-	32	-	nC
Gate-Source Charge	Q_{gs}		-	13.2	-	nC
Gate-Drain Charge	Q_{gd}		-	15.7	-	nC
Gate Plateau Voltage	$V_{plateau}$		-	7.2	-	V
Drain-Source Diode Characteristics [7]						
Body Diode Reverse Recovery Time	t_{rr}	I_F = 10A, dI/dt = 100A/μs, T_J = 25°C	-	379	-	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	5.1	-	μC
Body Diode Reverse Recovery Current	I_{rrm}		-	21	-	A
Diode Forward Current	I_S	T_C = 25°C	-	-	20	A

Notes:

1. This current is chip limited, which is calculated based on Rthjc.
2. This current is calculated on single pulse with 10μs Pulse & Duty Cycle = 1%.
3. Defined by design, not subject to production test, E_{AS} condition: T_J=25°C, V_{DD}=400V, V_{GS}=10V, L=50mH.
4. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
5. Thermal resistance from junction to the exposed pad).
6. Short duration pulse test used to minimize self-heating effect.
7. Defined by design, not subject to production.
8. $C_{O(er)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 480V.
9. $C_{O(tr)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 480V.

Typical Electrical and Thermal Characteristics

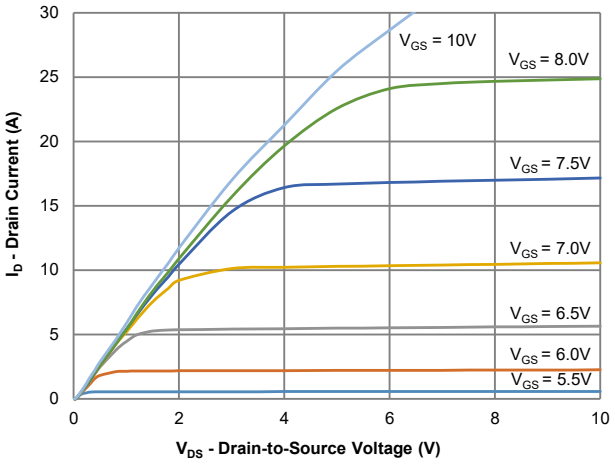


Figure 1: Output Characteristics

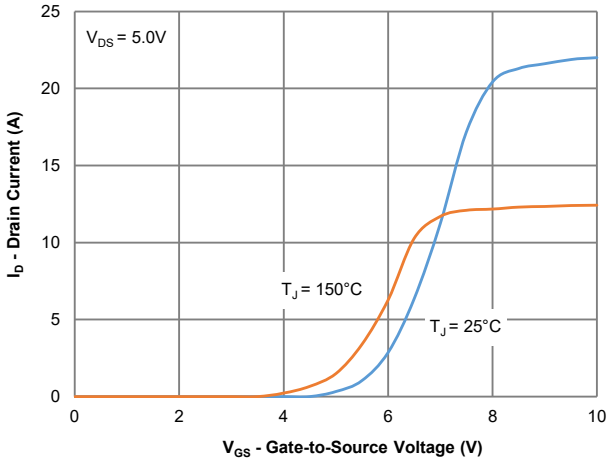


Figure 2: Transfer Characteristics

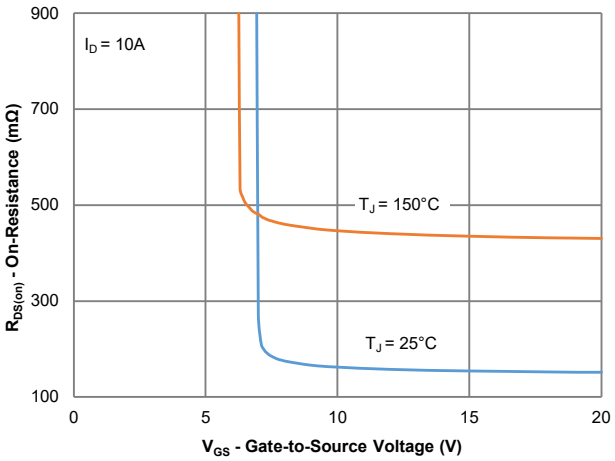


Figure 3: On-Resistance vs. Gate-Source Voltage

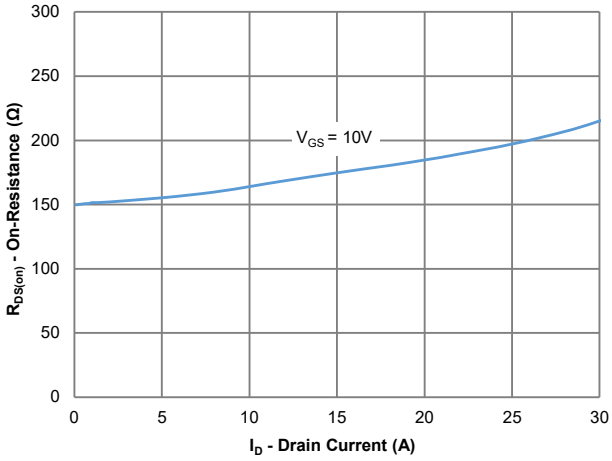


Figure 4: On-Resistance vs. Gate-Source Voltage

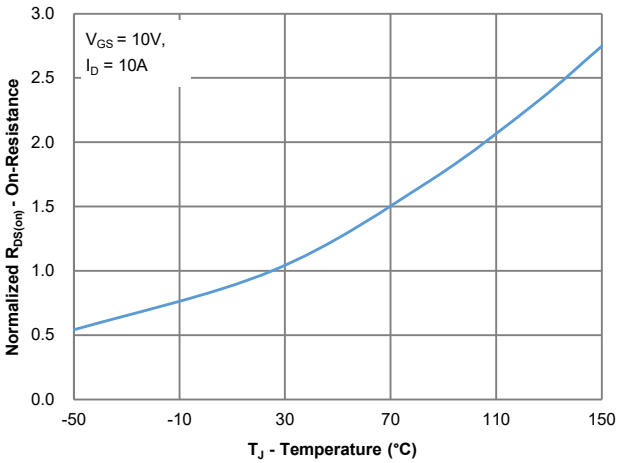


Figure 5: On-Resistance vs. Junction Temperature

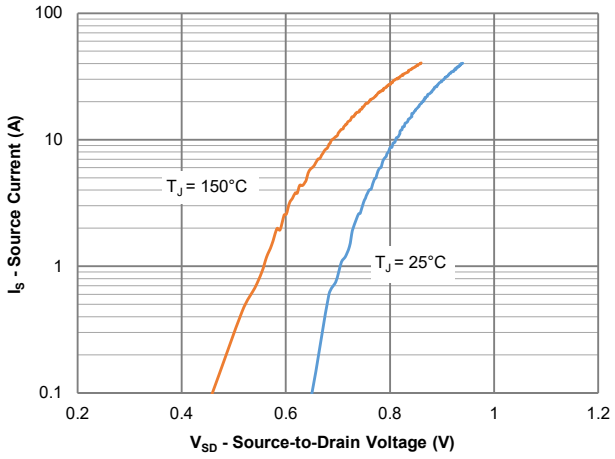


Figure 6: Source-Drain Diode Forward Voltage

Typical Electrical and Thermal Characteristics

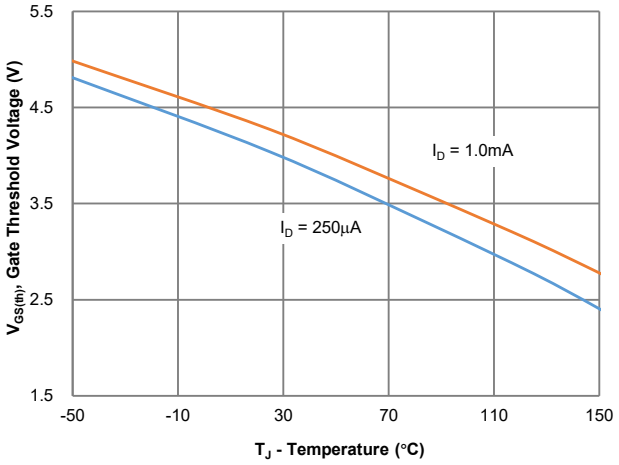


Figure 7: Gate Threshold Variation vs. Junction Temperature

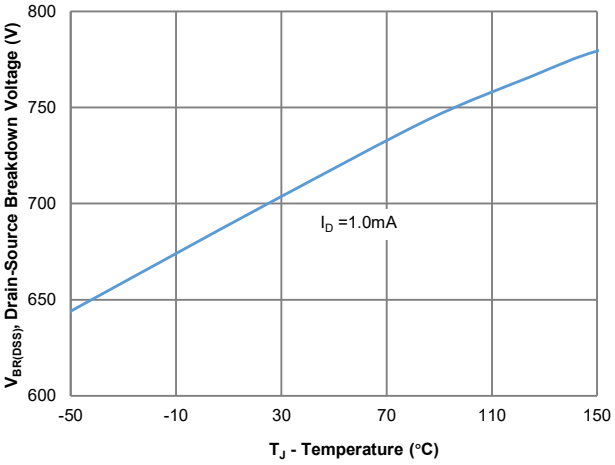


Figure 8: $V_{BR(DSS)}$ vs. Junction Temperature

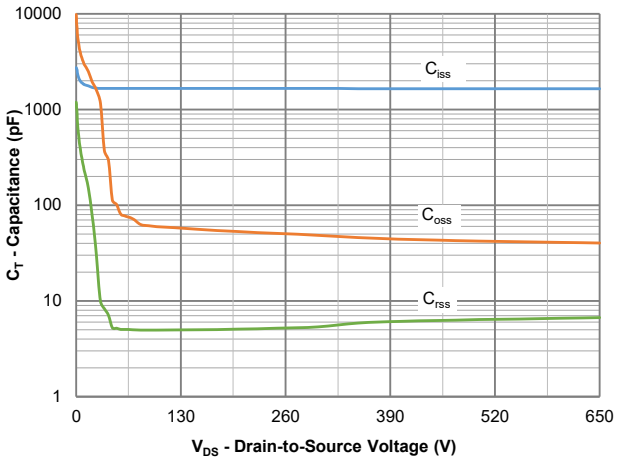


Figure 9: Capacitance Characteristics

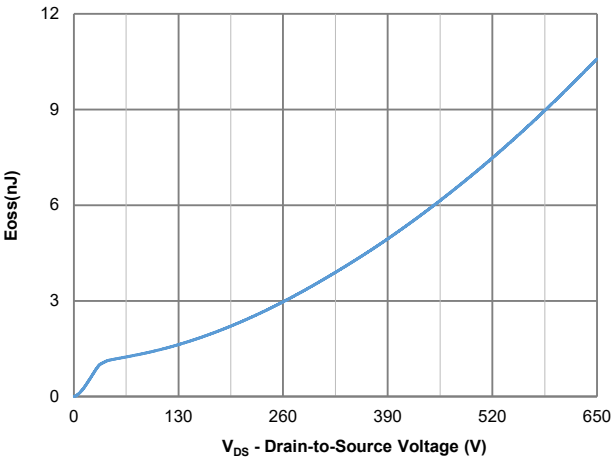


Figure 10: Coss Stored Energy

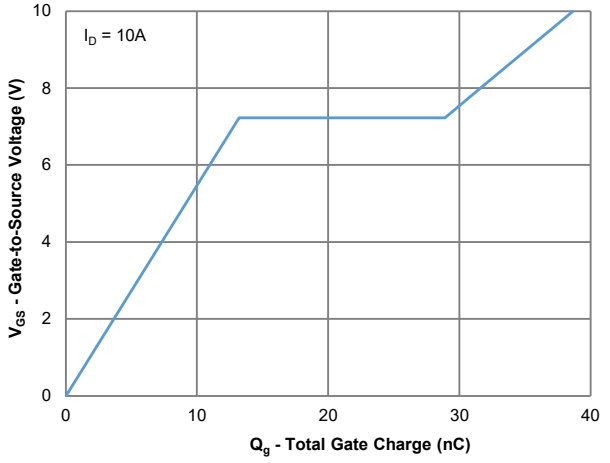


Figure 11: Gate Charge Characteristics

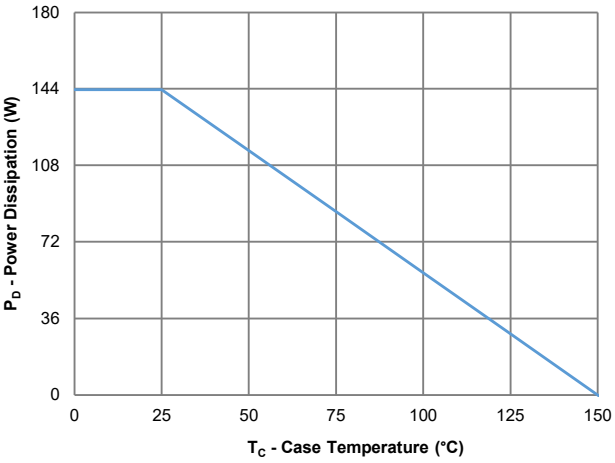


Figure 12: Power Derating

Typical Electrical and Thermal Characteristics

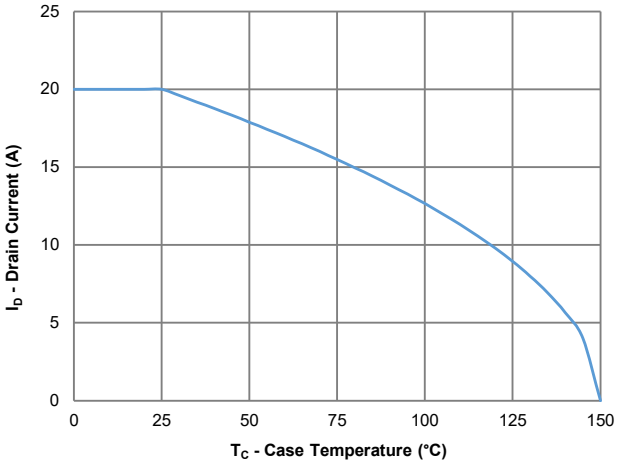


Figure 13: Current Derating

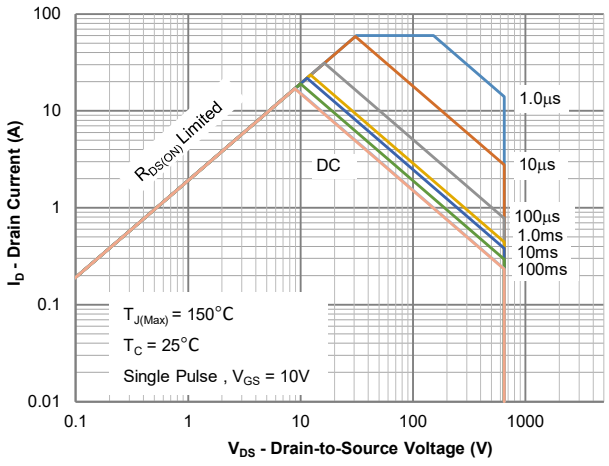


Figure 14: Safe Operating Area

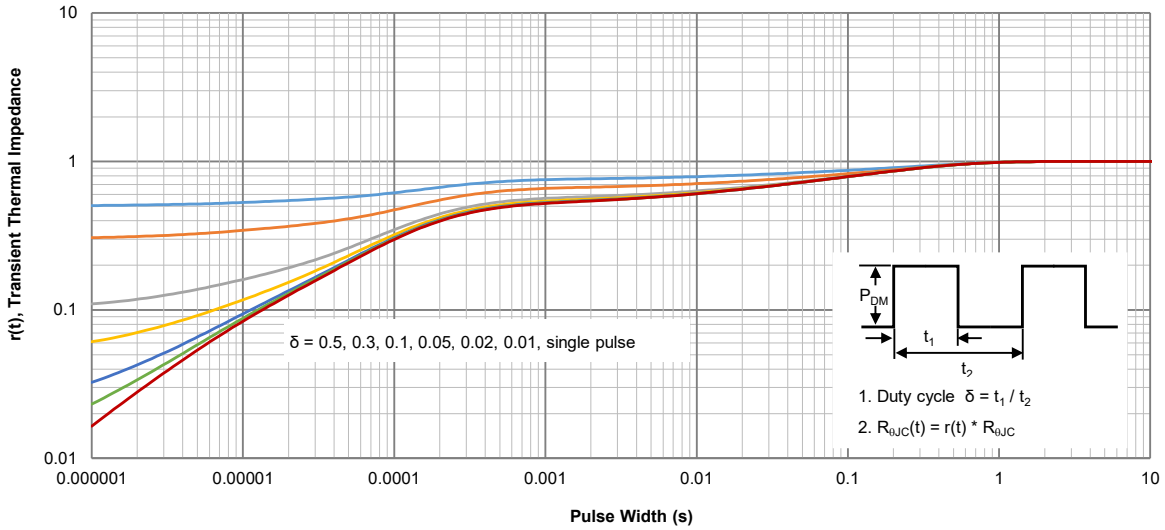
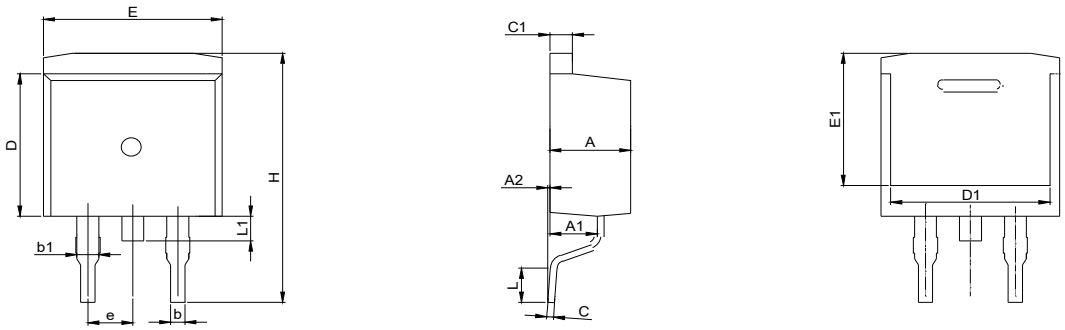
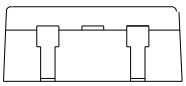


Figure 15: Normalized Maximum Transient Thermal Impedance

TO263-3L Package Outline

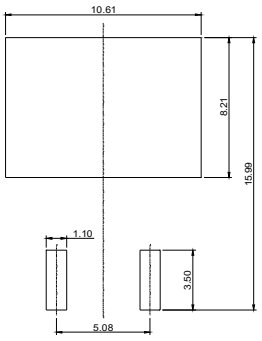




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMNESIONS IN MILLIMETER (ANNGLE IN DEGREE).
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH.

DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	4.20	4.50	4.70
A1	2.30	--	2.85
A2	0.00	0.10	0.25
b	0.70	0.80	0.95
b1	1.15	1.30	1.70
C	0.30	0.50	0.60
C1	1.15	1.30	1.42
H	14.00	15.20	15.88
D	8.50	9.20	9.60
D1	7.50	7.75	8.00
E	9.78	10.00	10.36
E1	7.60	7.95	8.10
L	1.50	--	2.50
L1	--	--	1.75
e	--	2.54	--

Recommended Footprint (Dimensions are in mm)



DIMENSIONS IN MILLIMETERS