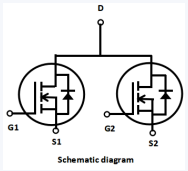
WAFER DATASHEET

Features

- $V_{(BR)DSS}$ = 20 V, I_D = 4.2 A
- $R_{DS(ON)}$ < 24 mΩ (max.) @ V_{GS} = 4.5 V
- $R_{DS(ON)}$ < 35 mΩ (max.) @ V_{GS} = 2.5 V
- Dual N-Channel, Common-Drain Configuration
- High Power and Current Handling Capacity
- Lead-Free Product
- For Surface Mount Packages

Applications

- PWM Application
- Load Switch
- Power Management



Schematic Diagram

Chip Information

Parameter	Value
Die Size (without scribe line)	961 µm × 602 µm (dual N)
Gate Pad Size	130 µm × 130 µm × 2
Source Pad Size	430 µm × 550 µm × 2
Scribe Line Size	60 µm
Wafer Thickness	150 µm
Wafer Diameter	300 mm, with (100) notch
Front Metal Composition & Thickness	AlCu, 4 µm
Back Metal Composition & Thickness	Ti-Ni-Ag, 1kÅ-2kÅ-10kÅ
Gross Die (approximately)	97,000

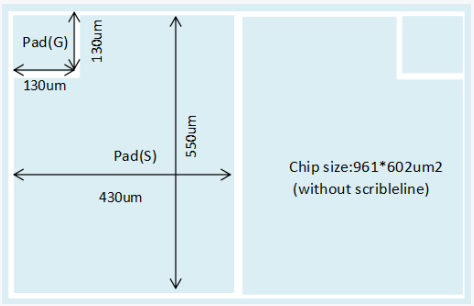


Diagram of chip

Ordering Information

Orderable Part Number	Product Form	Wafer Diameter	Shipping Option
SYN8205W3	Un-sawn Wafer	300 mm	Un-sawn wafer (standard)

Maximum Ratings (@ T_A = 25 °C, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Drain – Source Voltage	V_{DS}	20	V
Continuous Drain Current	I_D	4.2	A
Operating and Storage Temperature	T_J, T_{STG}	−55 ~ +150	°C

Electrical Characteristics (@ T_A = 25 °C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
Drain–Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	20	22.5	—	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	—	—	100	nA
Gate–Body Leakage Current	I_{GSS}	V_{GS} = ±12 V, V_{DS} = 0 V	—	—	±100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250 µA	0.5	0.7	1.0	V
Static Drain–Source On-Resistance (CP)	$R_{DS(ON)}$	V_{GS} = 4.5 V, I_D = 1 A	—	16.5	24	mΩ
		V_{GS} = 2.5 V, I_D = 1 A	—	20.5	35	mΩ

Shipping, Handling and Storage

Item	Requirement
Shipping	One shipping option is offered as standard: un-sawn wafer. Sampling CP test is performed in order to guarantee minimum yield.
Handling	Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263. Product must be handled only in a class 10,000 or better-designated clean room environment.
Wafer Storage	Proper storage conditions are necessary to prevent product contamination and/or degradation after shipment. Un-sawn wafers and singulated die can be stored for up to 12 months when in the original sealed packaging at room temperature (45% ± 15% RH controlled environment). Un-sawn wafers and singulated die that have been opened can be stored when returned to their containers and placed in a nitrogen purged cabinet, at room temperature (45% ± 15% RH controlled environment). Sawn wafers on a film frame are intended for immediate use and have a limited shelf life.

Notes

1. Electrical characteristics are referenced to the die assembled in a TSSOP-8 package. Bonding wire reference: Gate — Cu 1.65 mil × 2; Source — Cu 1.65 mil × 6 × 2.
2. (CP) Parameter verified by sampling chip-probe (wafer sort) test.
3. To reduce the risk of contamination or degradation, it is recommended that product not being used in the assembly process be returned to its original container and resealed with a vacuum seal process.