SYN8205W

20V Dual N-Channel Enhancement Mode MOSFET

WAFER DATASHEET

Features

- Power MOSFET
- Low Gate Charge
- Excellent $R_{DS(ON)}$

Applications

- Load Switch, Motor Driving
- DC-DC Converters
- Power Management Functions

Device Symbol

Chip Information

Parameter	Value
Die Size (include scribe line)	741 μm × 800 μm
Gate Pad Size	135 μm × 135 μm
Source Pad Size	Full Opening Area
Scribe Line Size	60 μm
Wafer Thickness	150 μm ± 15 μm
Wafer Diameter	200 mm
Front Metal Composition & Thickness	AlCu, 4 μm
Back Metal Composition & Thickness	Ti-Ni-Ag, 1kÅ-2kÅ-10kÅ
Passivation	SRO 6kÅ + SiN 5kÅ
Polyimide	NA
Gross Die (approximately)	100,000 (50,000 × 2)

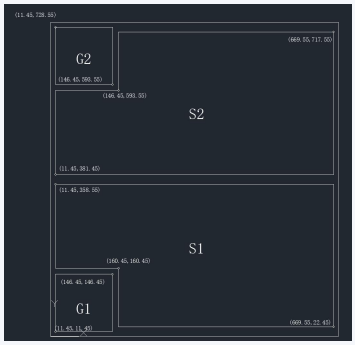

Diagram of chip

Maximum Ratings (@ T_A = 25 °C, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Drain – Source Voltage	V_{DS}	20	V
Gate – Source Voltage	V_{GS}	±12	V
Continuous Drain Current	I_D	6	A
Junction Temperature Range	T_J	−55 ~ +150	°C

Electrical Characteristics (@ T_A = 25 °C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
Drain–Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA	20	—	—	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V, T_J = 25 °C	—	—	1.0	μA
Gate–Body Leakage Current	I_{GSS}	V_{GS} = ±12 V, V_{DS} = 0 V	—	—	±100	nA
On Characteristics (1)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250 μA	0.4	0.6	0.9	V
Static Drain–Source On-Resistance (FT)	$R_{DS(ON)}$	V_{GS} = 4.5 V, I_D = 4 A	—	21	25.0	mΩ
		V_{GS} = 2.5 V, I_D = 3 A	—	26	30.0	mΩ
Static Drain–Source On-Resistance (CP)	$R_{DS(ON)}$	V_{GS} = 4.5 V, I_D = 1 A	—	—	25.0	mΩ
		V_{GS} = 2.5 V, I_D = 1 A	—	—	30.0	mΩ
Diode Forward Voltage	V_{SD}	I_S = 2.0 A, V_{GS} = 0 V	—	0.7	1.0	V

Notes

1. Measured under pulsed conditions. Pulse width ≤ 300 μs, duty cycle ≤ 2%.
2. $R_{DS(ON)}$ value is referred by the device assembled in SOT26.