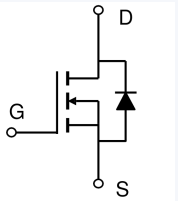
DATASHEET

## Features

- Low On-Resistance
- Excellent FoM (figure of merit)
- 100% UIS and $R_g$ tested

## Applications

- Load Switching
- Motor driver
- High frequency switching, synchronous rectification



Schematic Diagram

## Product Summary

| Parameter | Value | Unit |
|---|---|---|
| $V_{DS}$ | 40 | V |
| $R_{DS(on),TYP}$ @ $V_{GS}$=10V | 1.2 | mΩ |
| $I_D$ @$V_{GS}$=10V, T=25 °C | 212 | A |

## Ordering Information

| Orderable Part Number | Package Type | Device Marking | Form | Quantity (pcs) |
|---|---|---|---|---|
| QH4012AHP | PDFN5060-8L | QH4012AH | 13'' Tape&Reel | 5,000 |

## Maximum Ratings (@ $T_C$ = 25°C, unless otherwise specified.)

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Drain - Source Voltage | $V_{DS}$ | 40 | V |
| Gate - Source Voltage | $V_{GS}$ | ±20 | V |
| Continuous Drain Current ($V_{GS}$ = 10V) (1) $T_C$ = 25°C | $I_D$ | 212 | A |
| Continuous Drain Current ($V_{GS}$ = 10V) (1) $T_C$ = 100°C | | 134 | A |
| Pulsed Drain Current (2) | $I_{DM}$ | 850 | A |
| Single Pulse Avalanche Energy (3) | $E_{AS}$ | 436 | mJ |
| Single Pulse Avalanche Current (L= 0.1mH) | $I_{AS}$ | 56 | A |
| Power Dissipation $T_C$ = 25°C | $P_D$ | 104 | W |
| Power Dissipation $T_C$ = 100°C | | 42 | W |
| Junction & Storage Temperature Range | $T_J$, $T_{STG}$ | -55 ~ +150 | °C |

## Thermal Characteristics

| Parameter | Symbol | Typ. | Max. | Unit |
|---|---|---|---|---|
| Thermal Resistance, Junction-to-Ambient (4) | $R_{\theta JA}$ | 35 | 45 | °C/W |
| Thermal Resistance, Junction-to-Case (5) | $R_{\theta JC}$ | 0.9 | 1.2 | °C/W |

## Electrical Characteristics (@ $T_J$ = 25°C, unless otherwise specified.)

| Parameter | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Off Characteristics** (6) | | | | | | |
| Drain-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0V, $I_D$ = 250μA | 40 | — | — | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 40V, $V_{GS}$ = 0V | — | — | 1.0 | μA |
| | | $V_{DS}$ = 40V, $V_{GS}$ = 0V, $T_J$ = 125°C | — | — | 100 | μA |
| Gate-Source Leakage Current | $I_{GSS}$ | $V_{GS}$ = ±20V, $V_{DS}$ = 0V | — | — | ±100 | nA |
| **On Characteristics** (6) | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = 250μA | 2.0 | 3.0 | 4.0 | V |

| Parameter | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Static Drain-Source On-Resistance | $R_{DS(ON)}$ | $V_{GS}$ = 10V, $I_D$ = 20A | — | 1.2 | 1.4 | mΩ |
| Forward Transconductance | $g_{fs}$ | $V_{DS}$ = 5.0V, $I_D$ = 20A | — | 34 | — | S |
| Diodes Forward Voltage | $V_{SD}$ | $I_S$ = 2.0A, $V_{GS}$ = 0V | — | 0.7 | 1.2 | V |

## Dynamic Characteristics (7)

| Parameter | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = 20V, $V_{GS}$ = 0V, f = 1MHz | — | 3073 | — | pF |
| Output Capacitance | $C_{oss}$ | | — | 1515 | — | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | | — | 58 | — | pF |
| Gate Resistance | $R_g$ | $V_{GS}$ = 0V, $V_{DS}$ = 0V, f = 1MHz | — | 1.4 | — | Ω |

## Switching Characteristics (7)

| Parameter | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Turn-On DelayTime | $t_{d(on)}$ | $V_{GS}$ = 10V, $V_{DS}$ = 20V, $I_D$ = 20A, $R_{GEN}$ = 3.0Ω | — | 5.6 | — | ns |
| Rise Time | $t_r$ | | — | 15 | — | ns |
| Turn-Off DelayTime | $t_{d(off)}$ | | — | 20 | — | ns |
| Fall Time | $t_f$ | | — | 9.9 | — | ns |

## Gate Charge Characteristics (7)

| Parameter | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Total Gate Charge ($V_{GS}$ = 10V) | $Q_g$ | $V_{DS}$ = 20V, $I_D$ = 20A, $V_{GS}$ = 10V | — | 41 | — | nC |
| Total Gate Charge ($V_{GS}$ = 6.0V) | $Q_g$ | | — | 26 | — | nC |
| Gate-Source Charge | $Q_{gs}$ | | — | 14 | — | nC |
| Gate-Drain Charge | $Q_{gd}$ | | — | 7.5 | — | nC |
| Gate Plateau Voltage | $V_{plateau}$ | | — | 5.0 | — | V |

## Drain-Source Diode Characteristics (7)

| Parameter | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Body Diode Reverse Recovery Time | $t_{rr}$ | $I_F$ = 20A, dI/dt = 100A/μs, $T_J$ = 25°C | — | 46 | — | ns |
| Body Diode Reverse Recovery Charge | $Q_{rr}$ | | — | 50 | — | nC |
| Diode Forward Current | $I_S$ | $T_C$ = 25°C | — | — | 132 | A |

## Typical Electrical and Thermal Characteristics

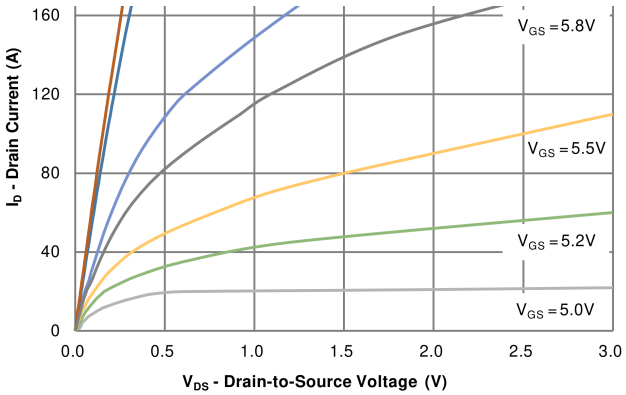



Figure 1: Output Characteristics

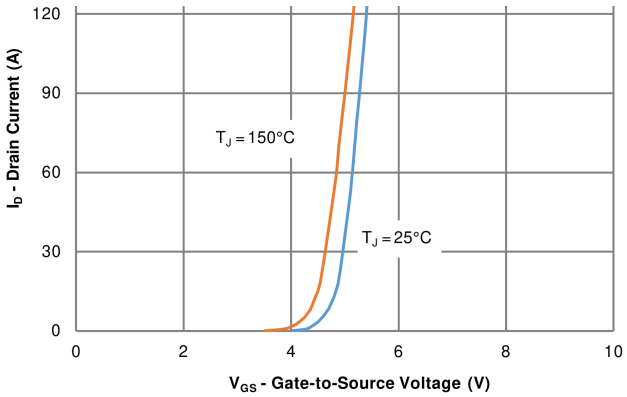



Figure 2: Transfer Characteristics

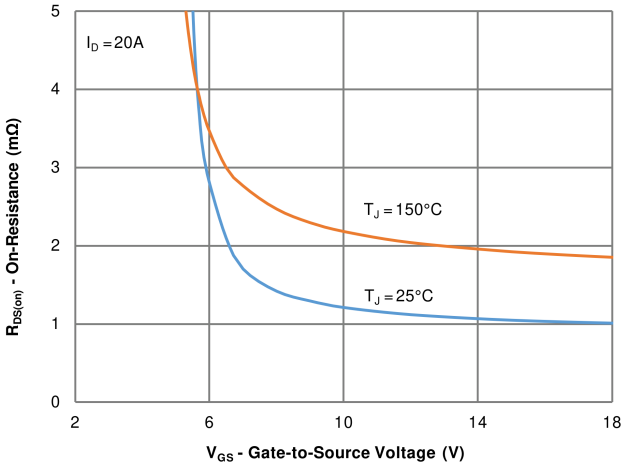



Figure 3: On-Resistance vs. Gate-Source Voltage

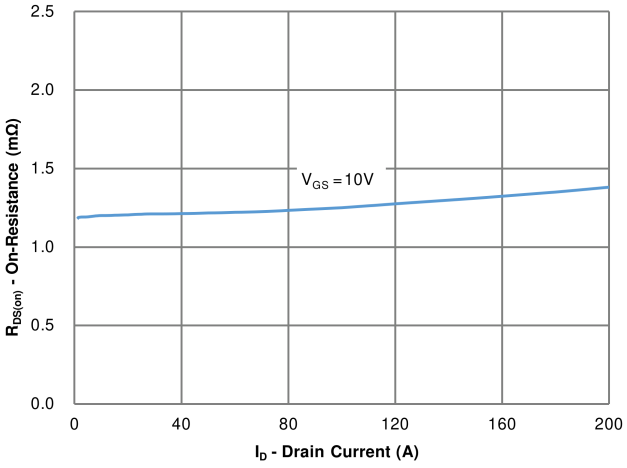



Figure 4: On-Resistance vs. Gate-Source Voltage

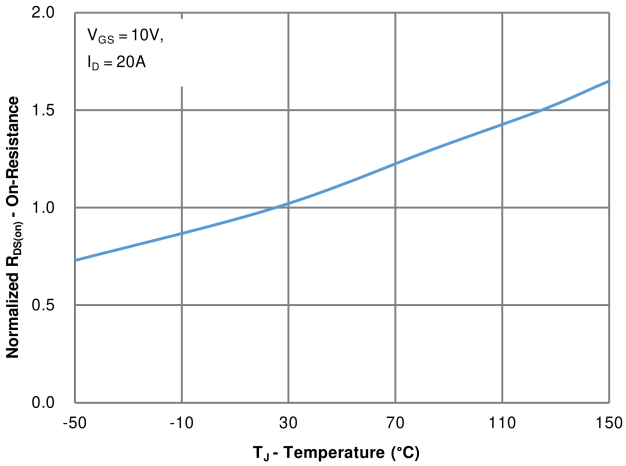



Figure 5: On-Resistance vs. Junction Temperature

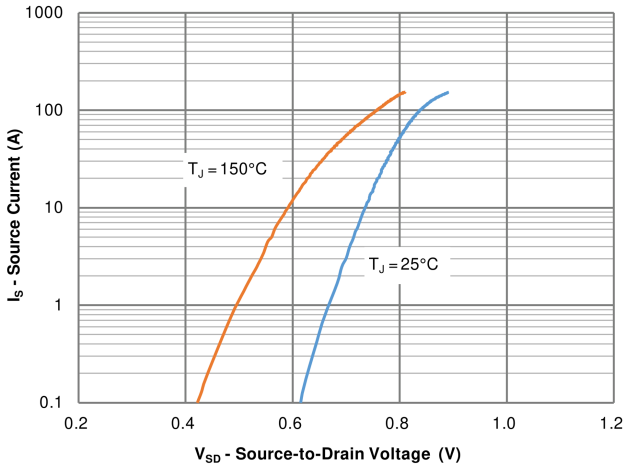



Figure 6: Source-Drain Diode Forward Voltage

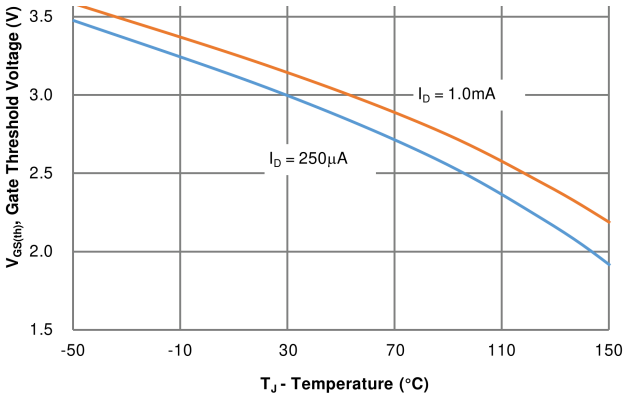



Figure 7: Gate Threshold Variation vs. Junction Temperature

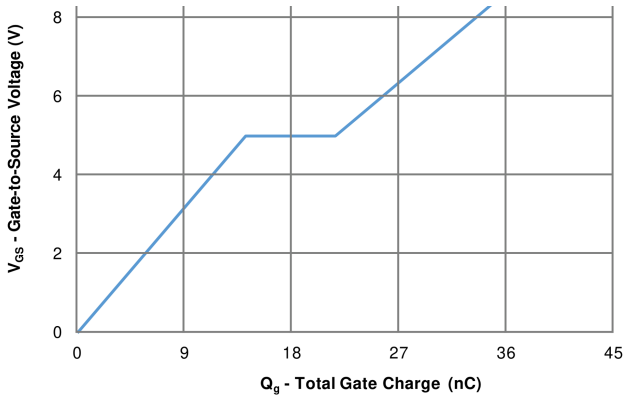



Figure 8: Gate Charge Characteristics

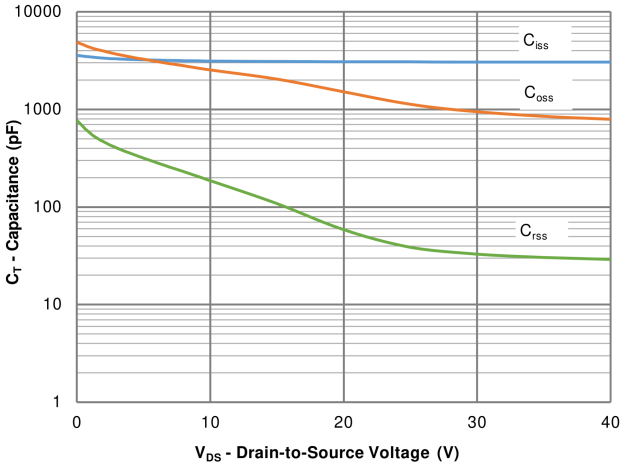



Figure 9: Capacitance Characteristics

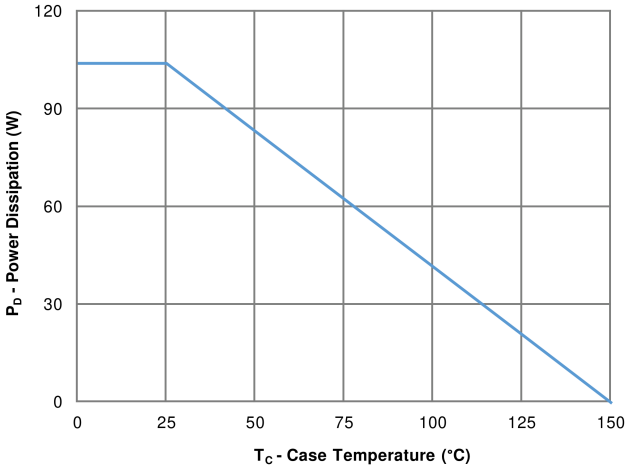



Figure 10: Power Derating

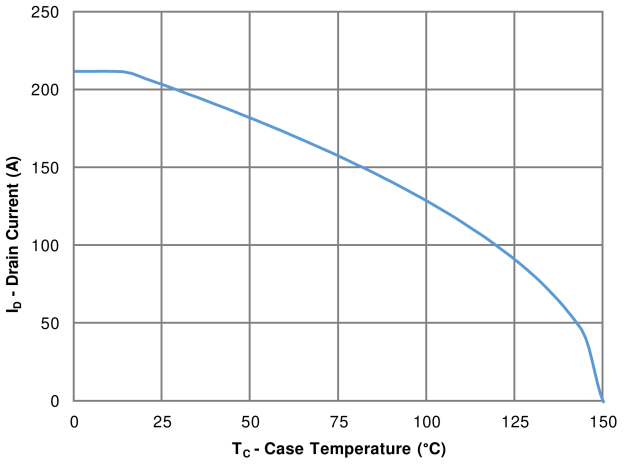



Figure 11: Current Derating

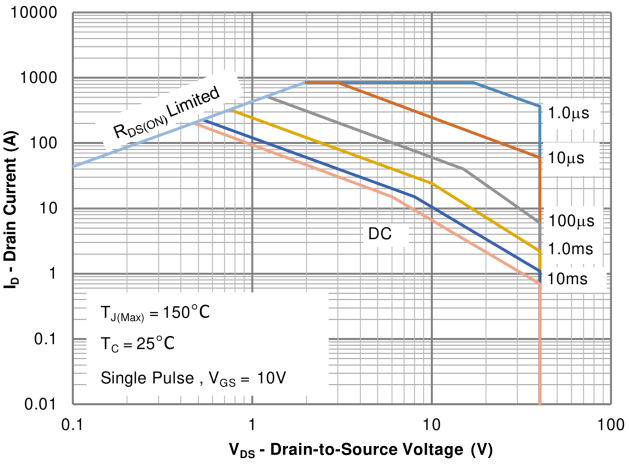



Figure 12: Safe Operating Area

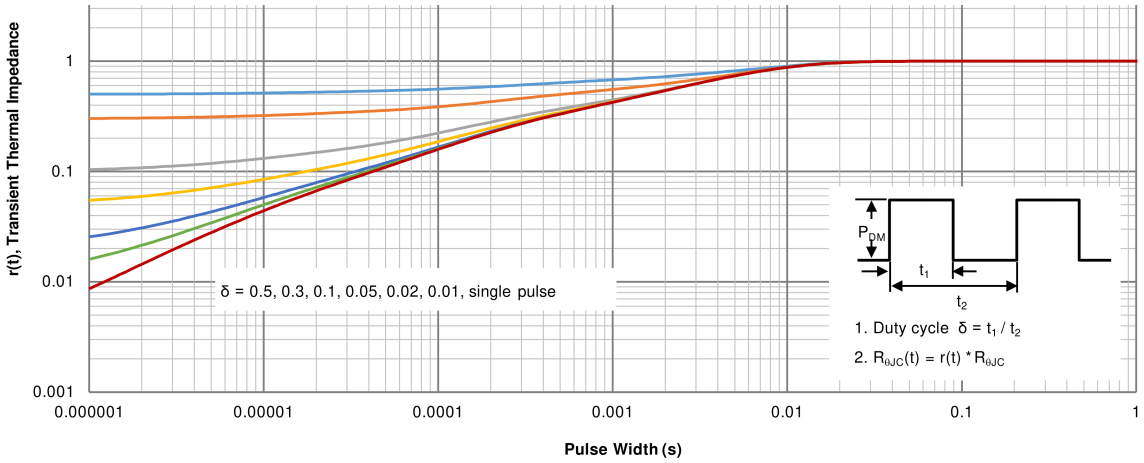
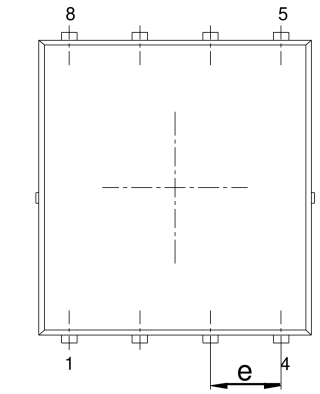


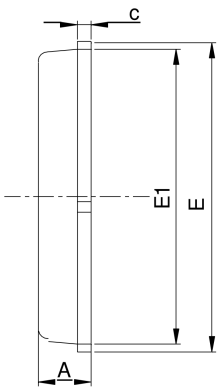

Figure 13: Normalized Maximum Transient Thermal Impedance

## PDFN5060-8L Package Dimensions

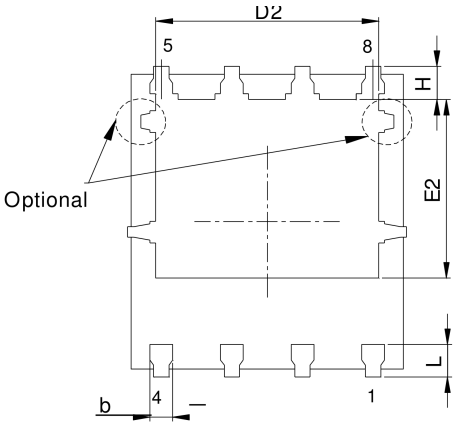
| DIM. | Min. | Nom. | Max. |
|---|---|---|---|
| A | 0.90 | 1.00 | 1.10 |
| b | 0.20 | — | 0.51 |
| c | 0.21 | 0.25 | 0.34 |
| D | 4.90 | — | 5.40 |
| D1 | 4.80 | — | 5.15 |
| D2 | 3.91 | — | 4.20 |
| E | 5.90 | — | 6.50 |
| E1 | 5.65 | 5.80 | 5.95 |
| E2 | 3.32 | 3.50 | 3.63 |
| e | | 1.27BSC | |
| H | 0.50 | — | 0.93 |
| L | 0.45 | — | 0.91 |
| θ | 0° | — | 12° |



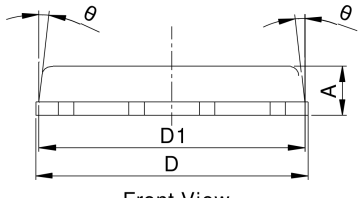
Top View



Side View



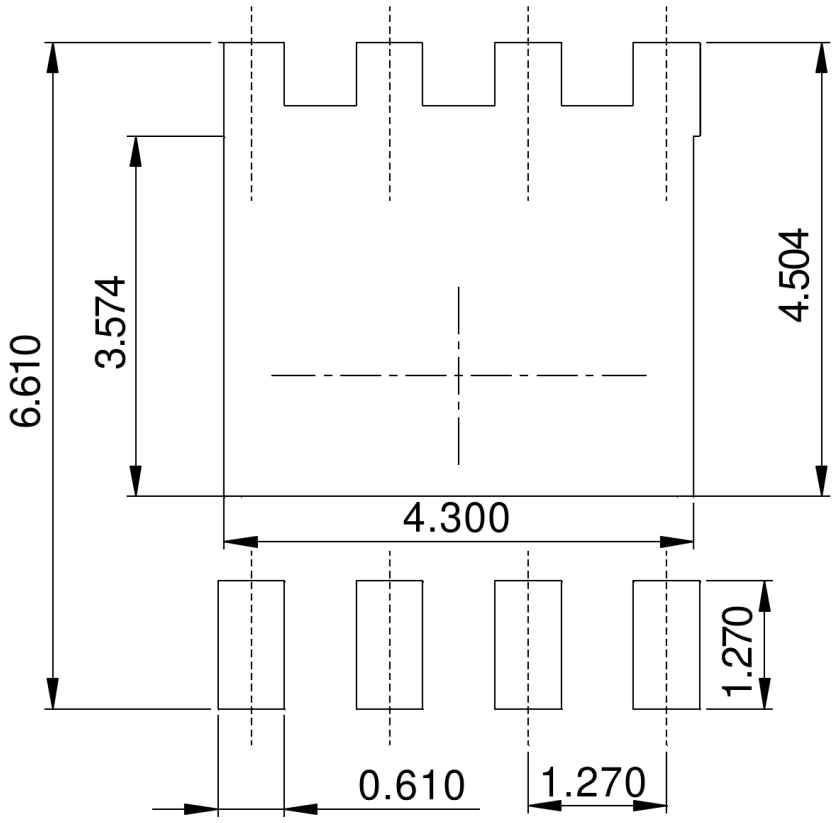
Bottom View



Front View

Dimensioning and tolerancing per ASME Y14.5M, 1994. All dimensions in millimeter (angle in degree). Dimensions D1 and E1 do not include mold flash protrusions or gate burrs.

## Recommended Soldering Footprint




DIMENSIONS:MILLIMETERS

**Notes**

1. This current is chip limited, which is calculated based on $R_{\theta JC}$.
2. This current is calculated on single pulse with 10µs Pulse & Duty Cycle = 1%.
3. Defined by design, not subject to production test, $E_{AS}$ condition: $T_J$=25°C, $V_{DD}$=20V, $V_{GS}$=10V, L=1.0mH.
4. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
5. Thermal resistance from junction to soldering point (on the exposed drain pad).
6. Short duration pulse test used to minimize self-heating effect.
7. Defined by design, not subject to production.