

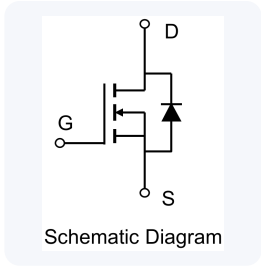
DATASHEET

Features

- Low On-Resistance
- Excellent FoM (figure of merit)
- 100% ΔV_{DS} & UIS & R_g tested

Applications

- Load switching
- Motor drives
- High frequency switching, synchronous rectification



Product Summary

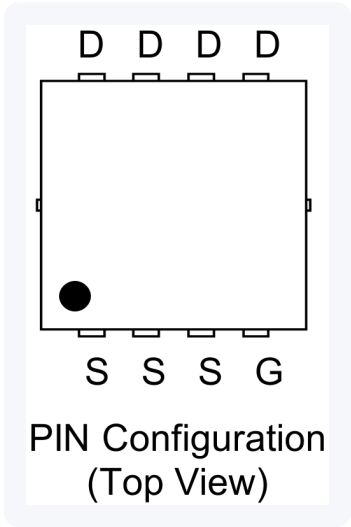
V_{DS}	$R_{DS(ON_TYP)}$	I_{D_MAX}
40 V	0.73 m Ω @ $V_{GS} = 10V$	314 A
	1.05 m Ω @ $V_{GS} = 4.5V$	

Mechanical Data

Green molding compound
Moisture sensitivity: level 1 per J-STD-020
UL flammability classification rating 94V-0

Pin Configuration

Pin #	Function	Symbol
1, 2, 3	Source	S
4	Gate	G
5, 6, 7, 8	Drain	D



Package PDFN5060-8L. Pin assignment per top-view pin configuration: pins 1–3 = Source, pin 4 = Gate, pins 5–8 = Drain.

Ordering Information

Orderable Part Number	Package Type	Device Marking	Form	Quantity (pcs)
4007ALPX	PDFN5060-8L	400SALX	13" Tape&Reel	5,000

Maximum Ratings (@ $T_C = 25^\circ\text{C}$, unless otherwise specified.)

Parameter	Symbol	Value	Unit
Drain - Source Voltage	V_{DS}	40	V
Gate - Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($V_{GS} = 10\text{V}$) ⁽¹⁾ $T_C = 25^\circ\text{C}$	I_D	314	A
Continuous Drain Current ($V_{GS} = 10\text{V}$) ⁽¹⁾ $T_C = 100^\circ\text{C}$		199	A
Pulsed Drain Current ⁽²⁾	I_{DM}	1257	A
Single Pulse Avalanche Energy ⁽³⁾	E_{AS}	1210	mJ
Single Pulse Avalanche Current ($L = 0.1\text{mH}$)	I_{AS}	85	A
Power Dissipation $T_C = 25^\circ\text{C}$	P_D	171	W
Power Dissipation $T_C = 100^\circ\text{C}$		68	W
Junction & Storage Temperature Range	T_J, T_{STG}	$-55 \sim +150$	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance, Junction-to-Ambient ⁽⁴⁾	$R_{\theta JA}$	32	40	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Case ⁽⁵⁾	$R_{\theta JC}$	0.67	0.73	$^\circ\text{C/W}$

Electrical Characteristics (@ $T_J = 25^\circ\text{C}$, unless otherwise specified.)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Off Characteristics ⁽⁶⁾						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	40	—	—	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}$	—	—	1.0	μA
		$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$	—	—	100	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	—	—	± 100	nA
On Characteristics ⁽⁶⁾						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1.2	1.7	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{V}, I_D = 20\text{A}$	—	0.73	0.95	m Ω
		$V_{GS} = 4.5\text{V}, I_D = 15\text{A}$	—	1.05	1.4	m Ω
Forward Transconductance	g_{fs}	$V_{DS} = 5.0\text{V}, I_D = 20\text{A}$	—	78	—	S
Diodes Forward Voltage	V_{SD}	$I_S = 2.0\text{A}, V_{GS} = 0\text{V}$	—	0.7	1.2	V

Dynamic Characteristics ⁽⁷⁾

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Capacitance	C_{iss}	$V_{DS} = 20\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	—	5508	—	pF
Output Capacitance	C_{oss}		—	2277	—	pF
Reverse Transfer Capacitance	C_{rss}		—	63	—	pF
Gate Resistance	R_g	$V_{GS} = 0\text{V}, V_{DS} = 0\text{V}, f = 1\text{MHz}$	—	0.80	—	Ω

Switching Characteristics ⁽⁷⁾

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Turn-On DelayTime	$t_{d(on)}$	$V_{GS} = 10\text{V}, V_{DS} = 20\text{V}, I_D = 20\text{A}, R_{GEN} = 3.0\Omega$	—	6.6	—	ns
Rise Time	t_r		—	13	—	ns
Turn-Off DelayTime	$t_{d(off)}$		—	55	—	ns
Fall Time	t_f		—	19	—	ns

Gate Charge Characteristics ⁽⁷⁾

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Total Gate Charge ($V_{GS} = 10V$)	Q_g		—	83	—	nC
Total Gate Charge ($V_{GS} = 4.5V$)	Q_g		—	40	—	nC
Gate-Source Charge	Q_{gs}	$V_{DS} = 20V, I_D = 20A, V_{GS} = 10V$	—	14.1	—	nC
Gate-Drain Charge	Q_{gd}		—	13.0	—	nC
Gate Plateau Voltage	$V_{plateau}$		—	2.8	—	V

Drain-Source Diode Characteristics ⁽⁷⁾

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 20A, dI/dt = 100A/\mu s, T_J = 25^\circ C$	—	57	—	ns
Body Diode Reverse Recovery Charge	Q_{rr}		—	84	—	nC
Diode Forward Current	I_S	$T_C = 25^\circ C$	—	—	314	A

Typical Electrical and Thermal Characteristics

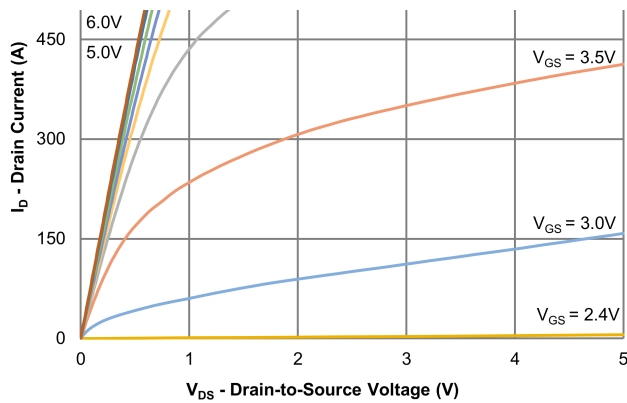


Figure 1: Output Characteristics

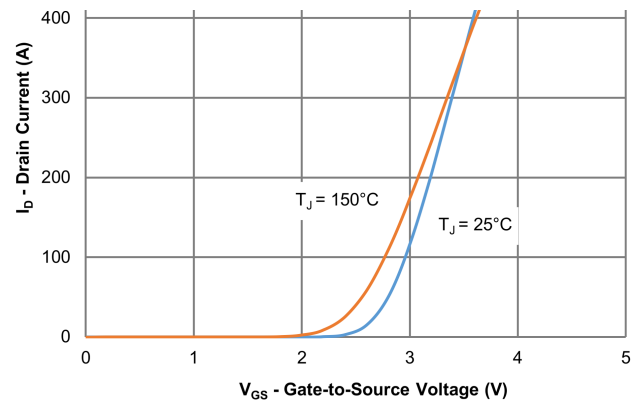


Figure 2: Transfer Characteristics

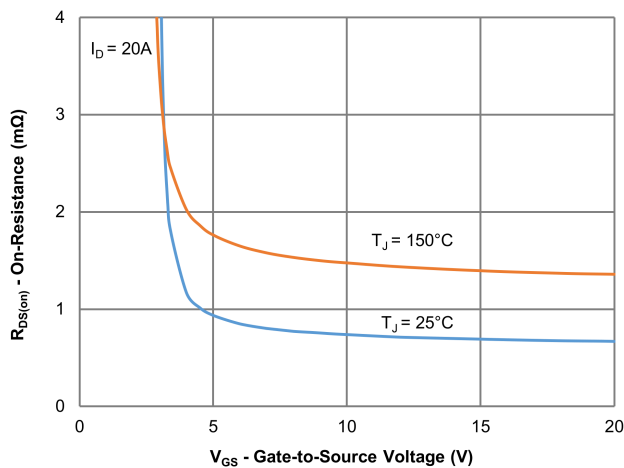


Figure 3: On-Resistance vs. Gate-Source Voltage

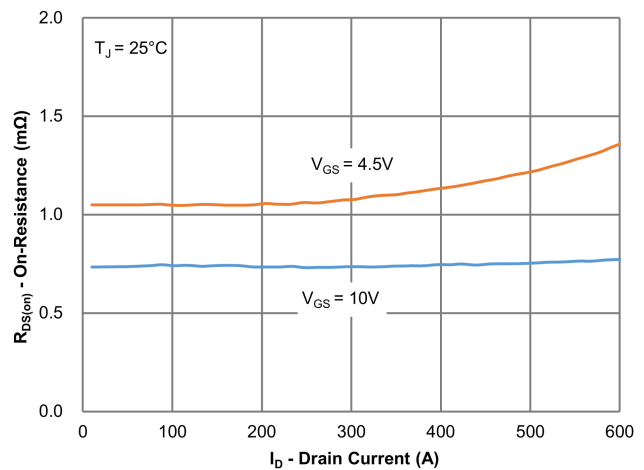


Figure 4: On-Resistance vs. Drain Current and Gate Voltage

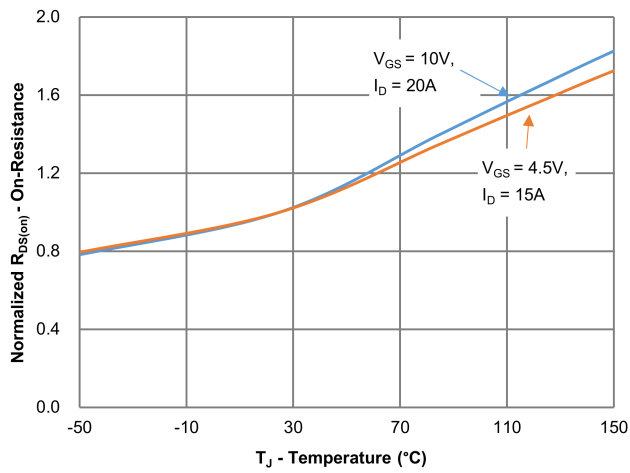


Figure 5: On-Resistance vs. Junction Temperature

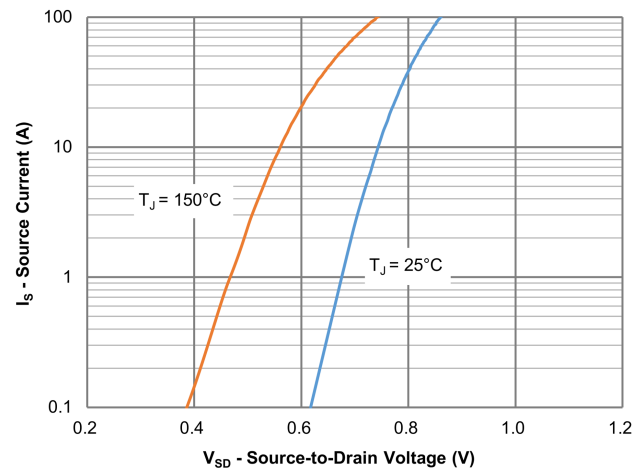


Figure 6: Source-Drain Diode Forward Voltage

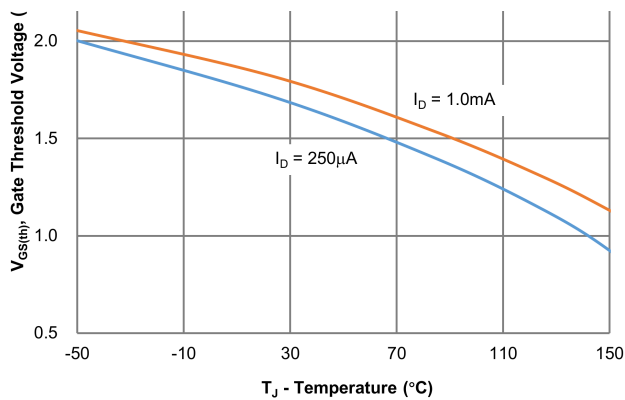


Figure 7: Gate Threshold Variation vs. Junction Temperature

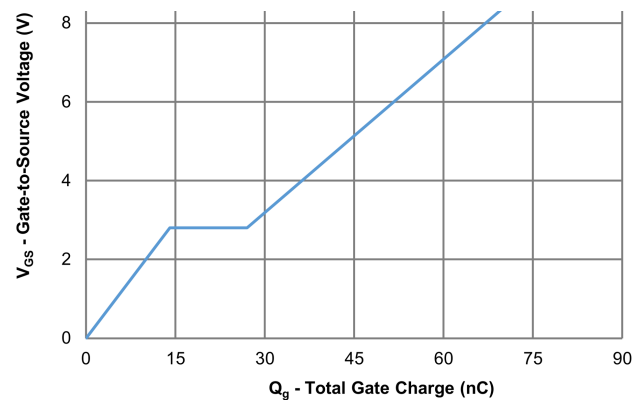


Figure 8: Gate Charge Characteristics

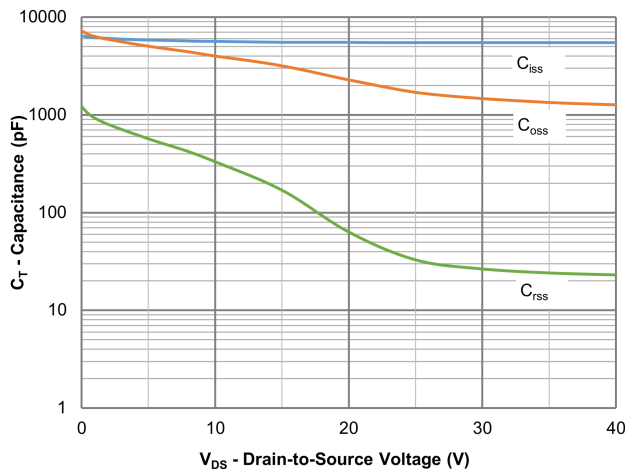


Figure 9: Capacitance Characteristics

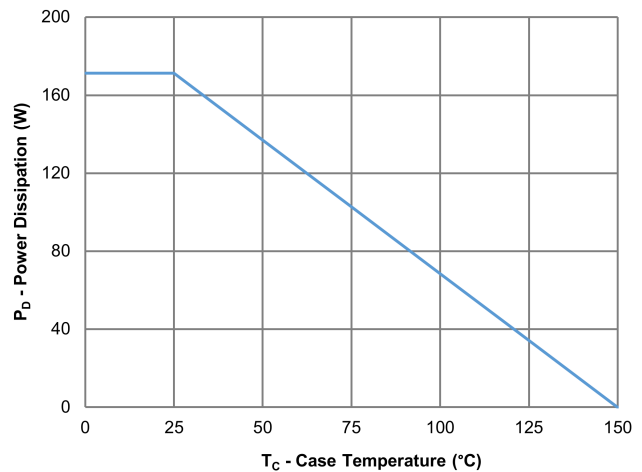


Figure 10: Power Derating

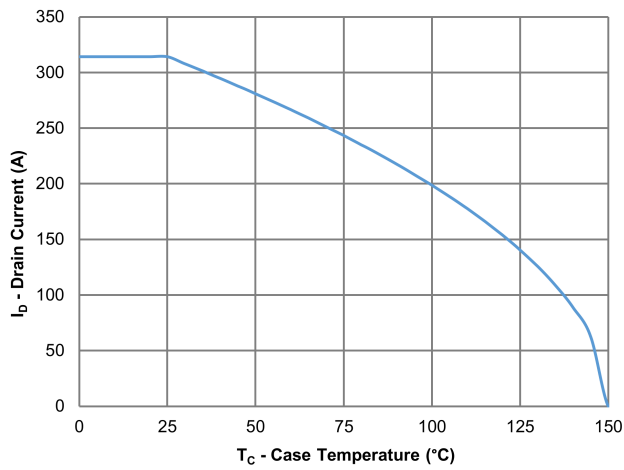


Figure 11: Current Derating

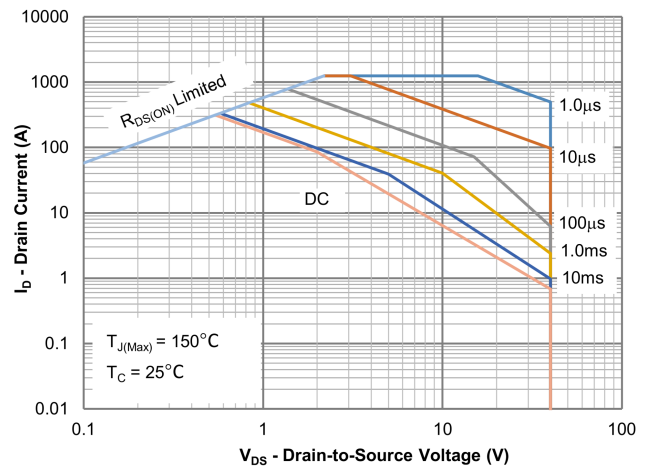


Figure 12: Safe Operating Area

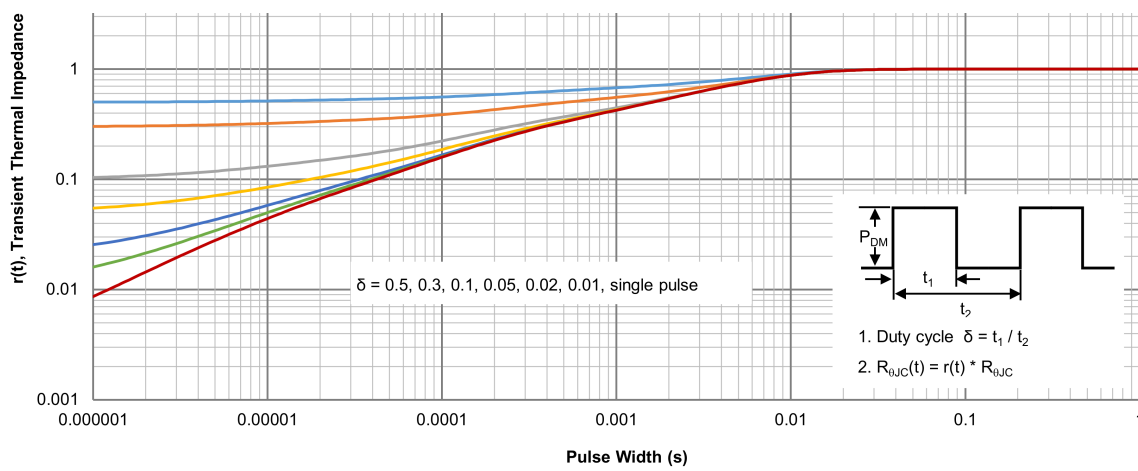
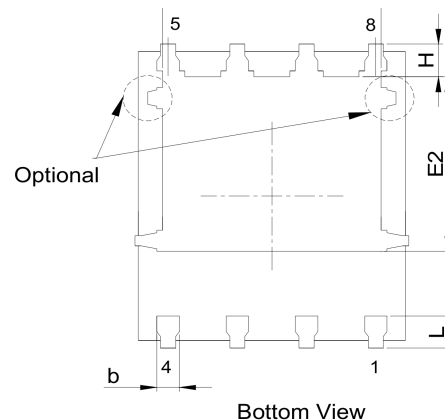
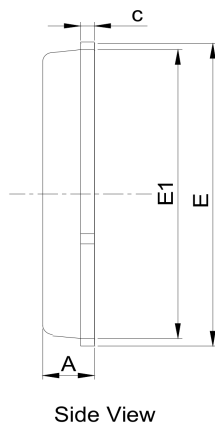
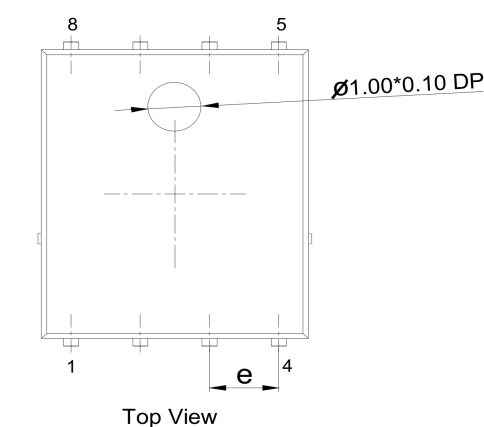


Figure 13: Normalized Maximum Transient Thermal Impedance

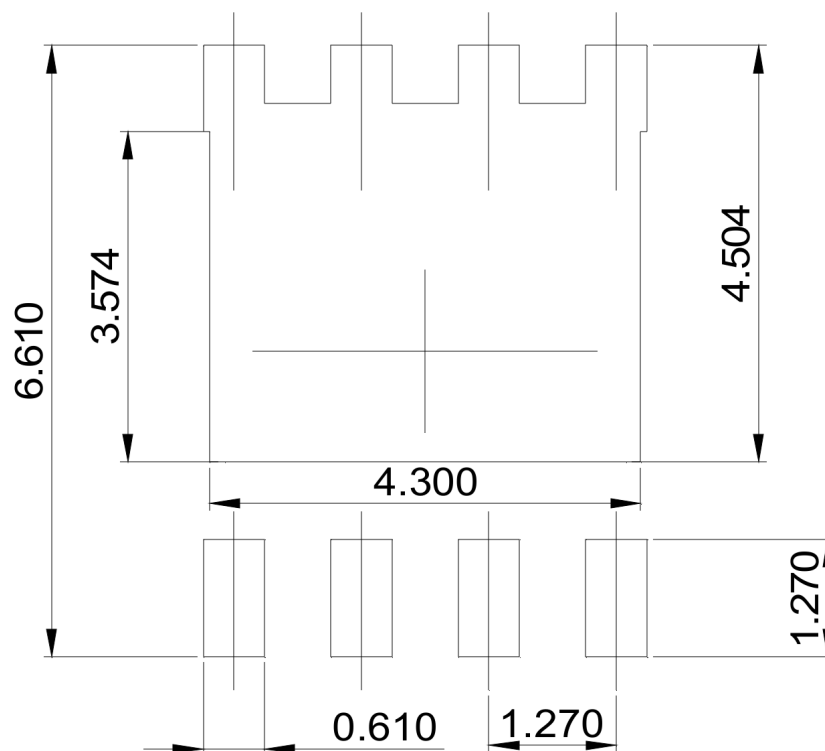
PDFN5060-8L Package Dimensions

DIM.	Min.	Nom.	Max.
A	0.90	1.00	1.10
b	0.20	—	0.51
c	0.21	0.25	0.34
D	4.90	—	5.40
D1	4.80	—	5.15
D2	3.70	—	4.20
E	5.90	—	6.50
E1	5.65	5.80	5.95
E2	3.32	3.50	3.63
e	1.27BSC		
H	0.50	—	0.93
L	0.45	—	0.91
θ	0°	—	12°



Dimensioning and tolerancing per ASME Y14.5M, 1994. All dimensions in millimeter (angle in degree). Dimensions D1 and E1 do not include mold flash protrusions or gate burrs.

Recommended Soldering Footprint



DIMENSIONS:MILLIMETERS

Notes

1. This current is chip limited, which is calculated based on $R_{\theta JC}$.
2. This current is calculated on single pulse with 10 μ s Single Pulse.
3. Defined by design, not subject to production test, E_{AS} condition: $T_J=25^{\circ}C$, $V_{DD}=20V$, $V_{GS}=10V$, $L=1.0mH$.
4. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
5. Thermal resistance from junction to the exposed pad.
6. Short duration pulse test used to minimize self-heating effect.
7. Defined by design, not subject to production.

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